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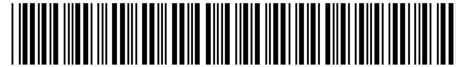

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(54) Gallium nitride-based III-V group compound semiconductor device and method of producing the same

Halbleitervorrichtung aus einer galliumnitridartigen III-V-Halbleiterverbindung und Verfahren zu ihrer Herstellung

Dispositif semi-conducteur composé III-V comprenant des composés à base de nitrure de gallium et procédé de fabrication

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Description

[0001] The present invention relates to a gallium nitride-based III-V Group compound semiconductor device, and a method of producing the same.

[0002] In recent years, a great deal of attention has been directed to light-emitting devices utilizing gallium nitride-based III-V Group semiconductors such as GaN, GaAlN, InGaN, and InAlGaN. Such a light-emitting device has a structure in which a layer of an n-type gallium nitride-based III-V Group compound semiconductor, and a layer of a gallium nitride-based III-V Group compound semiconductor doped with a p-type dopant are stacked on a substrate.

[0003] In the prior art, the layer of the gallium nitride-based III-V Group compound semiconductor doped with a p-type dopant remains as of high resistivity i-type. Therefore, the prior art device is of a so-called MIS structure. Recently, techniques to convert the high resistivity i-type compound semiconductor layer into a p-type layer has been disclosed in JP-A-2-257679, JP-A-3-218325, and JP-A-5-183189, and thus, it has now become possible to realize p-n junction type gallium nitride-based III-V Group semiconductor light-emitting devices, for example.

[0004] As such a p-n junction type gallium nitride-based III-V Group semiconductor devices have been being developed, it has become apparent that an electrode that is formed in direct contact with the p-type semiconductor layer or the n-type semiconductor layer has been encountered with various problems.

[0005] Presently, p-n junction type gallium nitride-based III-V Group semiconductor devices have a p-type compound semiconductor layer as the uppermost semiconductor layer due to the restriction imposed on the production thereof. Further, a transparent sapphire substrate is usually used for such a device. Different from a semiconductive substrate used for the other semiconductor light-emitting device, sapphire is electrically insulative. Thus, it is not possible to mount, directly on the substrate, electrodes for supplying a predetermined current to the compound semiconductor layer to cause the device to emit light. A p-electrode and n-electrode must be formed in direct contact with the p-type compound semiconductor layer and the n-type compound semiconductor layer, respectively. The p-electrode is usually formed to cover substantially entire surface of the p-type compound semiconductor layer in order to ensure the uniform application of current to the entire p-type compound semiconductor layer, thereby obtaining uniform light emission from the device. However, since the prior art p-electrode is not light-transmissive, the light emitted from the prior art light-emitting device must be observed on the side of the substrate, which is opposite to the side on which the compound semiconductor layers are formed.

[0006] Such a gallium nitride based III-V compound semiconductor LED is described in the article "ultraviolet and violet light-emitting GaN diodes grown by low-pressure metalorganic chemical vapor deposition" by B.Golden berg et al. in: Applied Physics Letters, vol. 62, No.4 (1993), pp. 381-383.

[0007] In mounting such a prior art compound semiconductor light-emitting device chip on lead frames, it is therefore necessary to place one such chip on two lead frames, with the p- and n-electrodes facing downward in order to direct upward the opposite side of the substrate on which no semiconductor layers are formed. In short, one device chip must be seated astride the two separate lead frames. In this case, the two lead frames must be set apart from each other at a certain distance in order to avoid electrical short-circuit between the p-type and n-type compound semiconductor layers, which inevitably leads to a large size of a device chip, such as 1 mm square or more. This results in the decrease in the number of chips which can be cut out from one semiconductor wafer. Further, very precise positioning of the two lead frames, and fine etching techniques for the gallium nitride-based compound semiconductors are required.

[0008] Next, an n-electrode will be described.

[0009] As mentioned above, it is in recent years that p-n junction type gallium nitride-based III-V Group compound semiconductor devices can be realized. In the prior art devices of a MIS structure, an electrode utilizes a Schottky barrier with the high-resistivity i-type semiconductor layer, and almost no attention is directed to the n-electrode.

[0010] As a material for an n-electrode in the prior art gallium nitride-based III-V Group compound semiconductor light-emitting device, aluminum or an alloy thereof is disclosed in, for example, JP-A-55-942. Also, indium is often used. However, it has been found that aluminum and indium can hardly establish an ohmic contact with the n-type gallium nitride-based III-V Group compound semiconductor layer, and tend to degrade by an annealing treatment, losing the electrical conductivity.

[0011] The object of the invention is to provide a new GaN-based III-V group compound semiconductor device having electrodes with improved properties, and methods of procuding the same.

[0012] This object is solved by the semiconductor devices comprising the features of claims 1 or 21, and by the methods according to clams 30 and 31, respectively. Advantageous embodiments of the invention are defined in the dependent claims.

[0013] In any event, there has been developed, in the prior art, no electrode materials that can establish a sufficiently satisfactory ohmic contact with a gallium nitride-based III-V Group compound semiconductor layers.

[0014] Therefore, it is a particular aspect of the present invention to provide a gallium nitride-based III-V Group compound semiconductor device provided with an electrode that establishes an ohmic contact with a gallium nitride-

based III-V Group compound semiconductor layer provided in the device, and a method of producing the same.

[0015] Another particular aspect of the present invention is to provide a gallium nitride-based III-V Group compound semiconductor device provided with a p-electrode that allows observation of the light emitted from the device to be made from a side of the substrate on which a gallium nitride-based III-V Group compound semiconductor layer is provided, and a method of producing the same.

[0016] Still another particular aspect of the present invention is to provide a gallium nitride-based III-V Group compound semiconductor device provided with an n-electrode that establishes an ohmic contact with an n-type gallium nitride-based compound semiconductor layer provided in the device, and a method of producing the same.

[0017] In one aspect of the present invention, there is provided a gallium nitride-based III-V Group compound semiconductor device, comprising:

a substrate;
a semiconductor stacked structure arranged over the substrate, and comprising an n-type gallium nitride-based III-V Group compound semiconductor layer and a p-type gallium nitride-based III-V Group compound semiconductor layer;
a first electrode provided in contact with the n-type semiconductor layer; and
a light-transmitting, second electrode provided in contact with the p-type semiconductor layer, and comprising a metallic material.

[0018] The second electrode (p-electrode) can be produced by forming a layer of a metallic material in contact with the p-type semiconductor layer, and annealing the metallic material layer, thereby rendering the metallic material layer light-transmissive and establishing an ohmic contact with the p-type semiconductor layer.

[0019] In a second aspect of the invention, a gallium nitride-based III-V Group compound semiconductor device, comprising:

a substrate;
a semiconductor stacked structure arranged over the substrate, and comprising an n-type gallium nitride-based III-V Group compound semiconductor layer and a p-type gallium nitride-based III-V Group compound semiconductor layer;
a first electrode provided in contact with the n-type semiconductor layer, and comprising titanium, and aluminum or gold; and
a second electrode provided in contact with the p-type semiconductor layer.

[0020] The first electrode (n-electrode) can be produced by forming, in contact with the n-type semiconductor layer, a metallic layer of an alloy containing titanium and aluminum or gold, or a multi-layered structure comprising a layer of titanium, and a layer of aluminum or gold, and annealing the metallic layer or multi-layered structure, thereby establishing an ohmic contact with the n-type semiconductor layer.

[0021] In a third aspect of the present invention, there is provided a gallium nitride-based III-V Group compound semiconductor device, comprising:

a substrate;
a semiconductor stacked structure arranged over the substrate, and comprising an n-type gallium nitride-based III-V Group compound semiconductor layer and a p-type gallium nitride-based III-V Group compound semiconductor layer;
a first electrode provided in contact with the n-type semiconductor layer, and comprising titanium, and aluminum or gold; and
a light-transmitting, second electrode provided in contact with the p-type semiconductor layer.

[0022] In a fourth aspect of the invention, there is provided a gallium nitride-based III-V Group compound semiconductor device, comprising a gallium nitride-based III-V Group compound semiconductor layer over a substrate, and an electrode which comprises a metallic material, and has been annealed so as to establish an ohmic contact with the semiconductor layer.

[0023] This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view, schematically illustrating a light-emitting device according to a first embodiment of the invention, with lead frames attached thereto;
FIG. 2 is a graph showing a current-voltage characteristic of a p-electrode of the invention, wherein one division of

X axis is 0.5 V, and one division of Y axis is 0.2 mA;

FIG. 3 is an oblique view illustrating a light-emitting device according to a second embodiment of the invention;
FIG. 4 is a cross-sectional view, taken along the line IV-IV of FIG. 3;
FIG. 5 is an oblique view illustrating a modification of the second embodiment of the invention;
FIG. 6 is a cross-sectional view illustrating a light-emitting device according to a third embodiment of the invention;
FIG. 7 is a cross-sectional view illustrating a first modification of the third embodiment of the invention;
FIG. 8 is a cross-sectional view illustrating a second modification of the third embodiment of the invention;
FIG. 9 is a cross-sectional view illustrating a third modification of the third embodiment of the invention;
FIG. 10 is a cross-sectional view illustrating a compound semiconductor light-emitting device according to a fourth embodiment of the invention;
FIGS. 11A to 11D are graphs showing current-voltage characteristics of different n-electrodes according to the invention, together with comparative examples, wherein one division of each X axis is 0.5 V, and one division of each Y axis is 50 μA;
FIGS. 12A to 12D are graphs showing current-voltage characteristics of different n-electrodes according to the invention, together with comparative examples, wherein one division of each X axis is 0.5 V, and one division of each Y axis is 50 μA;
FIGS. 13A to 13D are graphs showing current-voltage characteristics of different n-electrodes according to the invention, together with comparative examples, wherein one division of each X axis is 0.5 V, and one division of each Y axis is 50 μA;
FIGS. 14A to 14D are graphs showing current-voltage characteristics of different n-electrodes according to the invention, together with comparative examples, wherein one division of each X axis is 0.5 V, and one division of each Y axis is 50 μA;
FIG. 15 is a view for explaining a bonding test for n-electrodes;
FIG. 16 is a cross-sectional view partially illustrating a compound semiconductor light-emitting device according to a fifth embodiment of the invention; and
FIGS. 17A to 17D are graphs showing current-voltage characteristics of different n-electrodes in the fifth embodiment of the invention, together with comparative examples, wherein one division of each X axis is 0.5 V, and one division of each Y axis is 50 μA.

[0024] In the present invention, the term "gallium nitride-based III-V Group compound semiconductor" means a nitride semiconductor of a Group III element containing gallium, such as GaN, GaAlN, InGaN, or InAlGaN. Such a compound semiconductor may be represented by the formula:

$$In_xAl_yGa_{1-x-y}N$$

where $0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, and $x+y \leqq 1$.

[0025] In the present invention, the term "ohmic" is used in a sense ordinarily used in the field of semiconductors.

[0026] In the present invention, the term "light-transmitting", or "light-transmissive" with respect to an electrode means that the electrode transmits at least 1% of the light emitted from the gallium nitride-based III-V Group compound semiconductor light-emitting device therethrough, and does not necessarily mean colorless, transparent. A light-transmitting electrode usually transmits 20 to 40% or more of the light emitted from the device therethrough.

[0027] Further, in the present invention, when a metallic material comprises or contains two or more metals, these metals may be alloyed with each other in advance, or the metallic material may be of a multi-layered structure in which layers of the metals are sequentially stacked. When a metallic material contains two or more metals, the content of each metal is not particularly limited. However, it is preferred that the material contains at least 1 atomic % of each metal.

[0028] The present invention will now be described below in detail with reference to the accompanying drawing FIGURES. Throughout the FIGURES, the same parts or portions are denoted by the same reference numerals.

[0029] FIG. 1 schematically shows a gallium nitride-based III-V Group compound semiconductor light-emitting device 10 according to a first embodiment of the present invention.

[0030] The light-emitting device (LED) 10 has a transparent and electrically insulating substrate 11, such as sapphire. A layer 12 of an n-type gallium nitride-based III-V Group compound semiconductor is formed to a thickness of, for example, 0.5 μm to 10 μm, on a first major surface 11a of the substrate 11. The n-type semiconductor layer 12 is preferably doped with an n-type dopant, such as silicon (Si), germanium (Ge), selenium (Se), sulfur (S) or tellurium (Te), though an n-type dopant may not be doped thereinto.

[0031] On the surface of the n-type semiconductor layer 12, a layer 13 of a p-type gallium nitride-based III-V Group compound semiconductor is formed to a thickness of, for example, 0.01 μm to 5 μm. The p-type semiconductor layer 13 is doped with a p-type dopant, such as beryllium (Be), strontium (Sr), barium (Ba), zinc (Zn) or magnesium (Mg), and has been annealed at a temperature of 400°C or more (with respect to this annealing treatment, reference may be

made to JP-A-5-183189 filed by the present assignee, or U.S. Patent Application Serial No. 07/970,145 filed November 2, 1992, and assigned to the present assignee, which corresponds to EP-A-0,541,373).

[0032] The p-type semiconductor layer 13 is partially etched away, together with a surface portion of the n-type semiconductor layer, to partially exposing the surface of the n-type semiconductor layer 12. An n-electrode 14 is formed on the exposed surface portion of the n-type semiconductor layer 12.

[0033] A p-type electrode 15 of the invention is formed to directly cover a substantially entire surface of the p-type semiconductor layer 13. The p-electrode is a light-transmitting, ohmic electrode comprising a metallic material. The p-electrode may be formed of any suitable metallic material. The metallic material forming the p-electrode 15 may comprise one or more metals selected from gold, nickel, platinum, aluminum, tin, indium, chromium, and titanium. A metallic material achieving preferable ohmic characteristics contains at least two metals selected from chromium, nickel, gold, titanium and platinum. A particularly preferable metallic material contains gold and nickel. Gold and nickel are preferably formed such that a layer of nickel is formed in direct contact with the p-type semiconductor layer 13, and a layer of gold is formed on the nickel layer.

[0034] As mentioned before, where a metallic material for the p-electrode 15 contains two or more metals, these metals may be alloyed with each other in advance, or the metallic material may be of a multi-layered structure. The metals contained in the metallic material having such a multi-layered structure can form an alloy at an annealing treatment, which is described below.

[0035] The p-electrode 15 can be produced by forming a layer of a metallic material on the p-type semiconductor layer 13, using a conventional deposition technique, for example, vapor deposition or sputtering technique, and annealing the metallic material layer. The annealing treatment is preferably conducted at a temperature of 400°C or more. The metallic material layer tends not to establish a good ohmic contact with the p-type semiconductor layer 13, when it is annealed at a temperature below 400°C. Needless to say, the annealing treatment should be effected at a temperature below the decomposition temperature (around 1,200°C) of the gallium nitride-based III-V Group compound semiconductor. It is preferred that the annealing treatment in the present invention be conducted under a non-oxidative or inert atmosphere, such as nitrogen.

[0036] The effects of the annealing treatment performed on the p-electrode material are similar to those described in the above-mentioned USSN 07/970,145. That is, a gallium nitride-based III-V Group compound semiconductor grown by a vapor phase growth method and doped with a p-type dopant decreases in its resistivity, when it is annealed at a temperature of 400°C or more. This is because the hydrogen atoms bonded to the acceptor impurities in the as-grown compound semiconductor are expelled off by the annealing at 400°C or more, to activate the acceptor impurities. Thus, a carrier concentration in the compound semiconductor effectively increases to obtain a satisfactory ohmic contact, when the p-electrode material is annealed at a temperature of 400°C or more. A preferable p-electrode material which establishes a superior ohmic contact with the p-type semiconductor layer comprises nickel and gold, regardless of whether or not it is light-transmissive.

[0037] A metallic material used for the p-electrode 15 is preferably formed such that the annealed material has a thickness of 0.001 µm to 1 µm. During annealing, the metallic material layer partially diffuses into the p-type semiconductor layer 15, and is partially scattered outside. By adjusting the thickness of the final electrode to 0.001 µm to 1 µm, the p-electrode can be rendered light-transmissive. A thickness exceeding 1 µm may be used, but the metallic material layer tends to become more metallic-colored, lowering the light-transmissivity. From the light-transmitting point of view, p-electrode 15 is preferably thinner within the above thickness range. However, too small a thickness tends to increase the contact resistance between the electrode 15 and the p-type semiconductor layer 13. Accordingly, the thickness of the p-electrode 15 is more preferably 0.005 µm to 0.2 µm, and most preferably 0.01 µm to 0.2 µm.

[0038] The p-type electrode is light-transmissive, and establishes a preferable ohmic contact with the p-type semiconductor layer, lowering a forward voltage of the light-emitting device, thereby enhancing the light-emitting efficacy of the device.

Experiment 1

[0039] On a p-type GaN layer doped with zinc, a layer of nickel having a thickness of 0.1 µm, and then a layer of gold having a thickness of 0.1 µm were vapor-deposited, and annealed at 600°C to alloy them, preparing a light-transmitting p-electrode. The thickness of the electrode was 0.03 µm. The current-voltage characteristic of this p-electrode is shown by line A in FIG. 2. As seen from the FIGURE, this p-type electrode establishes a good ohmic contact with the p-type gallium nitride-based III-V Group compound semiconductor.

[0040] Returning to FIG. 1, the light-emitting device of the present invention having a light-transmissive, ohmic p-electrode 15 allows to observe the light emitted therefrom through the p-electrode 15. Therefore, as shown in FIG. 1, the device can be mounted on a cup-type lead frame 18 which is generally used for mounting a light-emitting device utilizing semiconductors other than gallium nitride-based III-V Group compound semiconductors. As shown, the bottom surface of the substrate, on which no semiconductor layers are formed, i.e., a second major surface 11b opposite to the

major surface 11a, is directed to the lead frame 18.

[0041] The p-type electrode 15 is connected with a bonding wire 21, such as a gold wire, at a bonding pad 17 formed on a portion of the surface of the p-type electrode 15. The bonding wire is, in turn, connected with a separate lead frame (metal post) 19. The n-electrode 14 is connected with the cup-like lead frame 18 through a bonding wire 20, such as a gold wire.

[0042] In a preferred embodiment of the present invention, the bonding pad 17 is preferably formed of gold alone, or a metallic material containing at least two metals including gold, and not containing aluminum or chromium. Such a metallic material may preferably comprise gold, and titanium, nickel, indium and/or platinum. These metallic materials exhibit a good adhesion with the p-electrode 13, and also exhibit a good adhesion with a metallic ball formed from a bonding wire during the wire bonding. Further, these metallic materials do not migrate into the p-electrode to degrade it (reduce the light-transmissivity) during the annealing treatment or during the application of the current to the device to emit light. A metallic material containing chromium or aluminum migrates into the p-electrode in a relatively short period of time (for example, 500 hours) during the application of the current, degrading the p-electrode.

Experiment 2

[0043] A bonding pad was formed on a p-electrode 15 of the device, as shown in FIG. 1, having a sapphire substrate as the substrate 15, a 4 μm thick n-type GaN layer as the n-type semiconductor layer 12, and a 1 μm thick p-type GaN layer doped with magnesium as the p-type semiconductor layer 13. The p-electrode 15 was produced by forming a nickel layer to a thickness of 0.1 μm and then a gold layer to a thickness of 0.1 μm, and annealing these layers at 600°C to alloy them and render the electrode light-transmissive. The thickness of the p-electrode thus formed was 0.05 μm.

[0044] Each bonding pad was formed from each of various metallic materials shown in Table 1 below such that a layer of a metal on the row of Table 1 was vapor-deposited directly on the p-electrode, and a layer of a metal on the line of Table 1 was vapor-deposited thereon. These metal layers were annealed simultaneously with the annealing of the p-electrode. The bonding wire was a gold wire.

[0045] Each device thus fabricated was caused to emit light continuously for 500 hours, and the influences of the bonding pad on the p-electrode were examined. The results are also shown in Table 1.

Table 1

Row \ Line	Au	Ni	Ti	In	Pt	Al	Cr
Au	VG	VG	G	G	G	B	B
Ni	VG	-	-	-	-	B	-
Ti	G	-	-	-	-	B	-
In	G	-	-	-	-	B	-
Pt	G	-	-	-	-	B	B
Al	B	B	B	B	B	B	B
Cr	B	-	-	-	-	B	-

[0046] In Table 1, the symbol, VG, stands for "very good", and indicates that the bonding pad remained light-transmissive, maintaining the initial light-transmissivity, and the ohmic property between the p-electrode and the p-type semiconductor layer was not changed. The symbol, G, stands for "good", and indicates that the portion of the p-electrode around the bonding pad is slightly color-changed, but not significantly attenuating the light form the device, and the ohmic property between the p-electrode and the p-type semiconductor layer was not changed. The symbol, B, stands for "bad", and indicates that the light-transmissivity of the p-electrode was lost, and also the ohmic property between the p-electrode and the p-type semiconductor layer was lost. The symbol "-" indicates that the bonding pad was poor in adhesion with the gold ball, and thus the wire bonding was difficult to perform.

[0047] As shown in Table 1, when the bonding pad is formed of the same metallic material as the p-electrode, i.e., Ni-Au, the p-electrode is not color-changed at all, and maintains the initial light-transmissivity. The same advantages are

obtained when the bonding pad is formed of gold. However, Cr or Al readily migrated into the p-electrode to degrade the characteristics of the p-electrode, even if gold was contained therein.

Experiment 3

[0048] Experiments were conducted in the same manner as in Experiment 2, except that the p-electrode was formed of Au-Ti (this p-electrode was slightly inferior to the Ni-Au electrode in the ohmic property). As a result, the bonding pad formed of gold alone or Au-Ti obtained the result of "VG". The bonding pad formed of gold and a metal other than aluminum or chromium (i.e., nickel, titanium, indium or platinum) obtained the result of "G". The bonding pad formed of a metallic material containing gold and aluminum or chromium obtained the result of "B".

Experiment 4

[0049] Experiments were conducted in the same manner as in Experiment 2, except that the p-electrode was formed of Au-Al (this p-electrode was slightly inferior to the Ni-Au electrode in its ohmic property). As a result, the bonding pad formed of gold alone obtained the result of "VG". The bonding pad formed of gold and a metal other than aluminum and chromium (i.e., nickel, titanium, indium or platinum) obtained the result of "V". However, the bonding pad formed of gold and aluminum obtained the result of "B", though it was the same material as the p-electrode. Further, the bonding pad formed of gold and chromium also obtained the result of "B".

[0050] FIG. 3 is a plan view of a semiconductor light-emitting device according to a second embodiment of the present invention. FIG. 4 is an enlarged cross-sectional view, taken along the line IV-IV of FIG. 3. This embodiment relates to an improvement in a bonding pad for the p-electrode. As shown in these FIGURES, a cut-off portion 311 is provided in the p-electrode 15, exposing a portion of the surface of the p-type semiconductor layer 13. A bonding pad 32 strongly adheres to the p-type semiconductor layer 13 through the cut-off portion 311, and is electrically connected with the p-electrode 15. In the embodiment shown, the bonding pad 32 not only fills the cut-off portion 311, but also extends over a portion of the p-electrode 15 around the cut-off portion 311. Preferably, the cut-off portion 311, and hence the bonding pad 32, are arranged farthest from the n-electrode 14 provided on the n-type semiconductor layer 12 (the same also applies to the device of FIG. 1). With such an arrangement, the applied current can spread throughout the entire p-type semiconductor layer 13 to obtain a uniform light output from the device. In the embodiment shown, the cut-off portion (window) 311 is arranged at a corner portion of the light-transmissive p-electrode 15, and the n-electrode 14 is arranged at an opposite corner portion of the n-type semiconductor layer 12, on a diagonal line of the square wafer.

[0051] Because the ohmic contact with the p-type semiconductor layer 13 is provided by the p-electrode 15, the bonding pad 32 may be formed of a metallic material which does not form an ohmic contact with the p-type semiconductor layer 13, though it may be formed of a metallic material establishing such an ohmic contact. The bonding pad 32 should be formed of a metallic material which adheres to the p-type semiconductor layer 13 more strongly than the p-electrode 15. Since the bonding pad 32 adheres to the p-type semiconductor layer 13 more strongly than the p-electrode 15, the bonding pad 13 and/or the p-electrode 15 is prevented from peeling off the substrate, even if the bonding pad 32 is pulled by a bonding wire, such as a gold wire, during the wire bonding operation. Such a material for the bonding pad includes aluminum alone, or a metallic material containing at least two metals selected from the group consisting of chromium, aluminum and gold. When a metallic material forming the bonding pad 32 contains two or more metals, these metals may be alloyed in advance, or the metallic material may comprises a layer of one metal, and a layer of the other metal stacked thereon, as mentioned before. The metals in the multi-layered structure can be simultaneously alloyed at time of the annealing treatment conducted on the p-electrode 15. These metallic materials may not establish a good ohmic contact with the p-type semiconductor layer 13, but strongly adheres to the p-type semiconductor material, and does not peel off from the wafer during the wire bonding operation. Therefore, these metallic materials may have so small a thickness as to be light-transmissive. Such a thin film bonding pad transmits the light emitted from the device therethrough, and does not significantly reduce the light output of the device. Further, the bonding pad 32 may be of a multi-layered structure in which a layer directly contacting the p-electrode 15 is formed of a metallic material which more strongly adheres to the p-type semiconductor layer 13, and the uppermost layer is formed of a metal which more strongly adheres to the material forming the bonding wire.

Experiment 5

[0052] 1,000 light-transmissive bonding pads were prepared on a p-type GaN layer by sequentially vapor-depositing a nickel layer and then a gold layer to a total thickness of 0.01 μm. On the other hand, each of Cr-Al, Al-Au, Cr-Au, and Al alone was vapor-deposited on a p-type GaN layer to a total thickness of 0.01 μm to provide 1,000 bonding pads on each p-type GaN layer. The bonding pads were bonded with corresponding gold wires, and the number of bonding

pads which were peeled off, when the gold wires were released, was counted to determine the yield of the bonding pads. The yield of the bonding pads formed of Ni-Au was about 60%, but the yield of each of the other bonding pads was 98% or more.

[0053] Meanwhile, the bonding strength with the p-type semiconductor layer 13 may be enhanced by making larger the thickness of the bonding pad 32. The thick bonding pad does not exhibit light-transmissivity, but may form an ohmic contact if formed of the same material as the p-electrode.

[0054] FIG. 5 shows a device similar to the device of FIG. 4, except that a cut-off portion 312 is provided such that a corner portion of the light-transmitting p-electrode 15 is cut away. In FIG. 5, the bonding pad filling the cut-off portion 312 is not shown, in order to clearly illustrate the cut-off portion 312.

[0055] FIG. 6 illustrate a light-emitting device according to a third embodiment of the invention, and shows a structure similar to the device of FIG. 1, except that an electrically insulating, transparent protective film (protective film 411) covers the thin, light-transmissive p-electrode 15. The protective film has a transparency such that it may transmit 90% or more of the light therethrough. The protective film is insulative, and thus prevents short-circuiting between the p-electrode 15 and the metallic ball that is formed on the n-electrode 14 during the wire bonding operation and remains there, even if the metallic ball is contacted with the p-electrode 15. Further, the protective film is transparent, and thus transmits the light emitted from the device therethrough. Accordingly, the protective film does not reduce the external quantum efficiency of the device. Further, the protective film protects the thin p-electrode 15 from being scratched, and prevents the bonding pad 17 or the p-electrode 15 from peeling off, even when pulled by the bonding wire during the wire bonding operation.

[0056] The material forming the protective film is not particularly limited, as long as it is transparent, and electrically insulative. A preferable material includes silicon oxide, titanium oxide, aluminum oxide, or silicon nitride. These materials are colorless, transparent, regardless of how thick it is formed, and are electrically insulative. Therefore, the protective films made of these materials does not substantially attenuate the light emitted from the device. The protective film can be formed by the conventional vapor deposition or sputtering technique. The thickness of the protective film is not particularly limited, but is usually 0.001 μm to 10 μm.

[0057] The metallic ball formed from the bonding wire tends to bridge the n-electrode 14 and the p-electrode 15 during the wire bonding operation at a region between the n-electrode 14 and the bonding pad 17. Therefore, the protective film 411 shown in FIG. 6 covers such a region entirely.

[0058] FIG. 7 shows a structure similar to the structure of FIG. 6, except that the protective film (protective film 412) covers the entire exposed surface of the p-electrode 15, the exposed edge surface of the p-type semiconductor layer 13, and the exposed surface of the n-type semiconductor layer 12. Therefore, the reliability of the device shown in FIG. 7 is more improved over that of the device of FIG. 6.

[0059] FIG. 8 shows a structure similar to the structure of FIG. 6, except that the protective film (protective film 413) continuously covers almost entire surface of the wafer excluding a bonding portion of the n-electrode 14, for bonding with a bonding wire, and a bonding portion of the bonding pad 17, for bonding with a bonding wire. By forming the protective film 413 also on the surface of the bonding pad 17, the bonding pad 17 becomes further pressed against the p-electrode 15, preventing the bonding pad 17 from peeling off the p-electrode 15. The protective film 413 also covers the n-electrode 14, preventing the n-electrode 14 from peeling off the n-type semiconductor layer 12. Thus, a device having a superior reliability is provided.

[0060] FIG. 9 shows a structure similar to the structure of FIG. 8, except that the n-electrode 14 and the bonding pad 17 are arranged at corner portions opposite to each other on a diagonal line of the square wafer. The advantages described with reference to FIG. 3 can also be obtained by this arrangement.

[0061] Next, an n-electrode of the present invention will be described.

[0062] An n-electrode according to the present invention is formed of a metallic material comprising titanium, and aluminum and/or gold, such as a metallic material containing titanium and aluminum, a metallic material containing titanium and gold, or a metallic material containing titanium, aluminum and gold. These metals may be alloyed in advance, or the metallic material may be of a multi-layered structure in which layers of the metals are sequentially stacked, as mentioned before. The n-electrode formed of such a metallic material establishes an excellent ohmic contact with an n-type gallium nitride-based III-V Group compound semiconductor layer when annealed.

[0063] The annealing temperature is particularly preferably 400°C or more. The annealing treatment is preferably conducted for 0.01 to 30 minutes, and under a non-oxidative or inert atmosphere such as nitrogen as described previously.

[0064] Generally, a gallium nitride-based III-V Group compound semiconductor has a property to become n-type without doping an n-type dopant thereinto, since nitrogen lattice vacancies are created in the grown crystal. The compound semiconductor exhibits a more preferable n-type conductivity when doped with an n-type dopant such as silicon, germanium, selenium, or sulfur. Gallium nitride-based III-V Group compound semiconductors are usually grown by a vapor phase growth method such as metalorganic chemical vapor deposition (MOCVD or MOVPE), hydride chemical vapor deposition (HDCVD), or molecular beam epitaxy (MBE). In such a growth method, compounds are used, which

contains hydrogen atoms, such as trimethylgallium as a gallium source, and ammonia or hydrazine as a nitrogen source, and also hydrogen gas as a carrier gas. The gaseous compounds which contain hydrogen atoms are thermally decomposed during the growth of the gallium nitride-based III-V Group compound semiconductor and release hydrogen. The released hydrogen atoms are trapped in the growing compound semiconductor, and combine with the nitrogen lattice vacancies or the n-type or p-type dopant, to inhibit their functions. It is believed that when the n-electrode material or the p-electrode material is annealed at a temperature of 400°C or more, the hydrogen trapped in the semiconductor crystal is expelled off, to activate the n-type or p-type dopant, thereby effectively increasing the electron carrier concentration or the hole carrier concentration in the semiconductor crystal, and establishing an ohmic contact. This effect of annealing is similar to the effect of annealing on a gallium nitride-based III-V Group compound semiconductor doped with a p-type dopant as described in the above-mentioned JP-A-5-183189 or USSN 07/970,145. These patent documents disclose that a gallium nitride-based III-V Group compound semiconductor doped with a p-type dopant gradually decreases in its resistivity starting from the annealing at 400°C, and exhibits a constant resistivity when annealed at 700°C or more. With the n-type gallium nitride-based III-V Group compound semiconductor of the present invention, the resistivity gradually decreases, starting from the annealing at 400°C, but does not show a sharp decrease. The n-type semiconductor exhibits a resistivity as low as 1/2 of the initial resistivity by the annealing treatment at 600°C, and no more decreases in its resistivity at a higher temperature.

[0065] The annealing is conducted on the n-electrode material preferably at 500°C or more, and more preferably 600°C or more. When the n-electrode material contains aluminum, a lower annealing temperature suffices, with 450°C or more being preferable, and 500°C or more being more preferable. The annealing should be conducted at a temperature lower than the decomposition temperature of the gallium nitride-based III-V Group compound semiconductor, as mentioned before. The thickness of the n-electrode is not particularly limited, but it is usually 5 nm or more, preferably 0.01 μm to 5 μm.

[0066] The n-electrode material of the invention comprising titanium, and aluminum and/or gold is preferably of a multi-layered structure in which layers of the metals are sequentially stacked. In this case, it is preferred that a layer of titanium be provided in direct contact with the n-type gallium nitride-based III-V Group compound semiconductor layer. Titanium can form a more preferable ohmic contact with the n-type gallium nitride-based III-V Group compound semiconductor layer. In such a case, the titanium layer is preferably formed to a thickness of 2 nm to 0.3 μm. A total thickness of the aluminum and/or gold layer subsequently formed is preferably larger than the thickness of the titanium layer. By forming the subsequent layer or layers to a such a total thickness, the titanium can be prevented from migrating onto the surface to lower the bonding strength of the n-electrode with the bonding wire or the metallic ball at the wire bonding.

[0067] An n-electrode material of the invention comprising titanium and gold, or comprising titanium, gold and aluminum has an anti-oxidation property improved over that of an n-electrode material comprising titanium and aluminum, and strongly adheres to the gold ball formed during the wire bonding. Further, an n-electrode material of the invention comprising gold preferably has a multi-layered structure in which a gold layer constitutes the uppermost layer. Naturally, the gold layer very strongly adheres to the gold ball.

[0068] FIG. 10 illustrates a light-emitting device according to a fourth embodiment of the invention, and shows a device of a double heterostructure having an n-electrode of the invention. This device has an n-type gallium nitride-based III-V Group compound semiconductor layer 51 having a thickness of, for example, 1 μm to 10 μm, formed over the substrate 11 through a buffer layer (not shown) formed of, for example, an undoped GaN having a thickness of 0.002 μm to 0.5 μm.

[0069] On the n-type semiconductor layer 51, a first clad layer 52 is provided, which is formed of an n-type gallium nitride-based III-V Group compound semiconductor, for example, an n-type GaAlN doped with an n-type dopant such as silicon. The first clad layer 52 usually has a thickness of 0.01 to 5 μm, preferably 0.1 to 4 μm.

[0070] On the first clad layer 52, an active layer (light-emitting layer) 53 is provided, which is formed of a gallium nitride-based III-V Group compound semiconductor having a semiconductor composition different from the clad layer 52. The active layer 53 is preferably formed of a low-resistivity $In_aGa_{1-a}N$, where $0 < a < 1$, doped with an n-type or p-type dopant, preferably an n-type dopant. The active layer 53 has a thickness of 1 nm to 0.5 μm, preferably 0.01 μm to 0.2 μm.

[0071] On the active layer 53, a second clad layer 54 is provided, which is formed of a p-type gallium nitride-based III-V Group compound semiconductor having a semiconductor composition different from the active layer 53, for example, a p-type GaAlN doped with a p-type dopant such as magnesium The second clad layer 54 has a thickness of, usually, 0.01 μm or more, preferably 0.1 μm to 1 μm.

[0072] On the second clad layer 54, a contact layer 55 is provided, which is formed of a p-type gallium nitride-based III-V Group compound semiconductor such as a p-type GaN.

[0073] A p-electrode 56 is provided on the contact layer 54. The p-type electrode 56 may be formed of any suitable, electrically conductive metallic material. A p-electrode material that exhibits a good ohmic property includes a metallic material comprising nickel and gold. Nickel and gold may be alloyed in advance. However, the metallic material com-

prising nickel and gold particularly preferably has a multi-layered structure in which a nickel layer and a gold layer are sequentially stacked. In the latter case, the nickel layer is preferably provided in direct contact with the contact layer 55. Of course, the light-transmitting p-electrode 15, and further the bonding pad 32, described with reference to the embodiments previously explained, may be applied to the device of FIG. 10. The p-electrode 56 is connected with a bonding wire 60 through a metallic ball 59.

[0074] The wafer shown is partially etched away from the contact layer 55 to a surface portion of the n-type semiconductor layer 51 in the direction of the thickness, partially exposing the n-type semiconductor layer 51. An n-electrode 57 of the present invention is provided on the exposed surface portion of the n-type semiconductor layer 51. The n-electrode 57 is connected with a bonding wire 61 through a metallic ball 58.

Experiment 6

[0075] An n-type GaN layer having a thickness of 4 μm was formed on a sapphire substrate having a diameter of 2 inches. On the n-type GaN layer, 1,000 n-electrodes having a diameter of 100 μm were vapor-deposited using each of various n-electrode material, and annealed at 450°C. The current-voltage characteristics were measured among the electrodes of the same material. The results are shown in FIGS. 11A to 11D. FIG. 11A relates to the 1,000 electrodes formed by depositing titanium and then aluminum at a thickness ratio of 0.01 : 1, and FIG. 11B relates to the 1,000 electrodes formed by depositing an Al-Ti alloy containing 1% by weight of titanium. FIG. 11C relates to the 1,000 electrodes formed by depositing titanium alone, and FIG. 11D relates to the 1,000 electrodes formed by depositing aluminum alone. These FIGURES show the representative results of the electrodes, respectively. As shown in FIGS. 11A and 11B, the electrodes comprising aluminum and titanium form a good ohmic contact with the n-type GaN layer. Each 1,000 electrodes all established a good ohmic contact with the n-type GaN as shown in FIGS. 11A and 11B. On the other hand, the electrodes formed of titanium alone or aluminum alone did not provide a good ohmic contact, as shown in FIGS. 11A and 11B, and, of these, only a few electrodes indicated the ohmic characteristics as shown in FIG. 11A or FIG. 11B.

[0076] Further, the electron microscopic observation indicated the electrodes formed of titanium alone or aluminum alone were blackened in 90% or more of their surface area.

Experiment 7

[0077] An n-type $Ga_{0.9}Al_{0.1}N$ layer having a thickness of 0.2 μm was formed on a sapphire substrate having a diameter of 2 inches. On the n-type GaAlN layer, 1,000 n-electrodes having a diameter of 100 μm were formed by vapor-depositing a multi-layered metallic material comprising a titanium layer and an aluminum layer, with the thickness ratio of the titanium and aluminum layer varied, and annealing them at 450°C. The current-voltage characteristics were measured among the electrodes of the same material. The results are shown in FIGS. 12A to 12D. FIG. 12A relates to the 1,000 electrodes formed by depositing the titanium layer and then the aluminum layer at a thickness ratio of 0.001 : 1, and FIG. 12B relates to the 1,000 electrodes formed by depositing the aluminum layer and then the titanium layer at a thickness ratio of 0.001 : 1. FIG. 12C relates to the 1,000 electrodes formed by depositing the titanium layer and then the aluminum layer at a thickness ratio of 1 : 0.001, and FIG. 12D relates to the 1,000 electrodes formed by depositing the aluminum layer and then the titanium layer at a thickness ratio of 1 : 0.001. These FIGURES show that all the electrodes formed of titanium and aluminum exhibit good ohmic characteristics, regardless of the ratio of titanium and aluminum contained in the electrode. Further, all the Ti-Al electrodes in which the titanium layer was formed in direct contact with the n-type semiconductor layer exhibited the good ohmic characteristics as shown in FIGS. 12A and 12B, but some of the Al-Ti electrodes in which the aluminum layer was formed in direct contact with the n-type semiconductor layer did not exhibit preferable ohmic characteristics. The electron microscopic observation indicated all the electrodes prepared in this Experiment were not degraded.

Experiment 8

[0078] On an n-type GaAlN layer doped with silicon, a titanium layer having a thickness of 0.03 μm was first vapor-deposited, then an aluminum layer having a thickness of 0.5 μm was vapor-deposited, and finally a gold layer having a thickness of 0.5 μm was vapor-deposited. The multi-layered structure was annealed at various temperatures for 5 minutes. The current-voltage characteristics were measured on the electrodes thus obtained. The results are shown by lines A to D in FIGS. 13A to 13D, respectively. FIG. 13A relates to the annealing at 300°C, FIG. 13B relates to the annealing at 400°C, FIG. 13C relates to the annealing at 500°C, and FIG. 13D relates to the annealing at 600°C. As seen from these FIGURES, the electrode did not exhibit preferable ohmic characteristics with the n-type semiconductor layer, when annealed at 300°C (FIG. 13A), but the electrodes exhibited preferable ohmic characteristics when annealed at 400°C or more (FIG. 13B to FIG. 13D). The similar results were obtained when the n-electrode was prepared by

depositing an alloy of titanium and aluminum.

Experiment 9

[0079] Experiments were conducted as in the same manner as in Experiment 8, except that a titanium layer having a thickness of 0.03 μm was vapor-deposited on the n-type GaN layer doped with silicon, and then a gold layer having a thickness of 0.5 μm was vapor-deposited. The results are shown by lines A to D in FIGS. 14A to 14D, respectively. FIG. 14A relates to the annealing at 300°C, FIG. 14B relates to the annealing at 400°C, FIG. 14C relates to the annealing at 500°C, and FIG. 14D relates to the annealing at 600°C. As seen from these FIGURES, the electrode did not exhibit preferable ohmic characteristics with the n-type semiconductor layer, when annealed at 300°C (FIG. 14A), but the electrodes exhibited preferable ohmic characteristics when annealed at 400°C or more (FIG. 14B to FIG. 14D). The similar results were obtained when the n-electrode was prepared by depositing an alloy of titanium and gold.

[0080] It can be understood from the comparison of FIGS. 13A to 13D with FIGS. 14A to 14D that when aluminum is added to a metallic material containing titanium and gold, the resultant electrodes exhibits a preferable ohmic characteristics even when annealed at a lower temperature. The fact that preferable ohmic characteristics can be obtained at a lower annealing temperature brings about advantages that the thermal decomposition of gallium nitride-based III-V Group compound semiconductors can be suppressed, and thus their crystallinity can be maintained.

Experiment 10

[0081] The following experiments were conducted to determine the bonding strength between an n-electrode and a gold ball.

[0082] Referring to FIG. 15, 100 thin films of Al, or 100 multi-layered films of Ti-Al, Ti-Au, Ti-Au-Al or Ti-Al-Au, each having a diameter of 120 μm, were formed on an n-type GaN layer 61 doped with silicon, and annealed at 500°C to prepare n-electrodes 62. The electrodes was subjected to a surface-oxidation by allowing them to stand in air for a day. Then, a gold wire 64 was ball-bonded to each electrode 62. A gold ball 63 having a diameter of 100 μm was formed during this operation. The ball 63 was clawed with an edged tool 65 from just beside the ball in a horizontal direction, while applying a load, until the ball 63 was peeled off, or crushed without peeling off. The results are shown in Table 2. In Table 2, the value under each load value column indicates the number of the balls peeled off the electrodes. It is indicated "crushed" where the ball was not peeled off, but was crushed.

Table 2

Material \ Load	20g	30g	40g	50g	60g	70g
Al	95	5	-	-	-	-
Ti-Al	93	7	-	-	-	-
Ti-Au-Al	0	0	6	25	69	-
Ti-Al-Au	0	0	0	1	5	crushed
Ti-Au	0	0	0	0	1	crushed

[0083] As shown in Table 2, the n-electrode formed of titanium and gold, or titanium, aluminum and gold has an anti-oxidation property improved over the electrode formed of titanium and aluminum, and thus exhibits a higher bonding strength with the gold ball. Further, it is seen that, of the n-electrodes formed of titanium, aluminum and gold, a higher adhesion strength can be obtained when the uppermost layer is formed of gold, than when the uppermost layer is formed of aluminum.

[0084] In order to prevent the bonding strength, with the metallic ball, of an n-electrode material containing titanium and aluminum from lowering due to the oxidation, it is also preferable to cover the surface of the n-electrode material with a layer of a high-melting point metallic material having a melting point higher than aluminum. Such a high-melting point metallic material includes gold, titanium, nickel, platinum, tungsten, molybdenum, chromium and/or copper, with gold, titanium and/or nickel being most preferred. These materials exhibit a superior adhesion with a first metallic material layer containing titanium and aluminum, and do not separate from the first metallic material layer. Further, these metallic materials strongly bond with the metallic ball formed during the wire bonding. Most preferably, the high-melting

point metallic material contains gold. A particularly preferable high-melting point metallic material contains gold and a high-melting point metallic material other than gold (preferably titanium and/or nickel). The high-melting point metallic material may be alloyed in advance, but is preferably of a multi-layered structure in which layers of the metals are sequentially stacked. In the latter case, the uppermost layer is preferably formed of gold, as mentioned before. After the stacked layer structure was formed, an annealing treatment is conducted under the above-mentioned conditions to obtain an n-electrode. The high-melting point metallic material prevents the aluminum contained in the underlying, first metallic material from migrating onto the surface, thereby preventing the oxidation of the aluminum.

[0085] FIG. 16 shows an n-electrode 57 of such a multi-layered structure. In FIG. 16, the n-electrode 57 has a fist thin film 57a of a multi-layered structure comprising a titanium layer and an aluminum layer, and formed on the n-type semiconductor layer 51. A second thin film of, for example, a multi-layered structure comprising layers of the high-melting point metallic materials is provided on the first thin film 57a.

Experiment 11

[0086] Experiments were conducted as in the same manner as in Experiment 8, except that a titanium layer having a thickness of 0.03 μm was vapor-deposited on the n-type GaN layer doped with silicon, and then an aluminum layer having a thickness of 0.1 μm was vapor-deposited, thus forming a first thin film, and further a titanium layer having a thickness of 0.03 μm was vapor-deposited on the aluminum layer, then a nickel layer having a thickness of 0.03 μm was vapor-deposited, and finally a gold layer having a thickness of 0.5 μm was vapor-deposited, thus forming a second film. The results are shown by lines A to D in FIGS. 17A to 17D, respectively. FIG. 17A relates to the annealing at 300°C, FIG. 17B relates to the annealing at 400°C, FIG. 17C relates to the annealing at 500°C, and FIG. 17D relates to the annealing at 600°C. As seen from these FIGURES, the electrode did not exhibit preferable ohmic characteristics with the n-type semiconductor layer, when annealed at 300°C (FIG. 17A), but the electrodes exhibited preferable ohmic characteristics when annealed at 400°C or more (FIG. 17B to FIG. 17D). It is also seen that the annealing at 600°C did not degrade the ohmic characteristics of the electrode.

Experiment 12

[0087] In order to determine the bonding strength of an n-electrode with a gold ball, experiments were conducted in the same manner as in Experiment 10, using electrode materials shown in Table 3 below. The results are also shown in Table 3.

Table 3

Material \ Load	20g	30g	40g	50g	60g	70g
Ti-Al	93	7	-	-	-	-
Ti-Al-Au	0	0	0	1	5	crushed
Ti-Al-Ti-Au	0	0	0	0	0	crushed
Ti-Al-Ni-Au	0	0	0	0	0	crushed
Ti-Al-Ti-Ni-Au	0	0	0	0	0	crushed

[0088] As seen from Table 3, the high-melting point metallic material improves the anti-oxidation property of the metallic material containing titanium and aluminum, and enhances the bonding strength with the gold ball.

[0089] It should be noted that the n-electrode of the present invention, as described so far, can be applied as the n-electrode 14 of any of the devices of FIG. 1, and FIGS. 3 to 9, thereby improving their device characteristics.

[0090] The present invention will be described below by way of the following Examples.

Example 1

[0091] A wafer was prepared, which had a buffer layer (thickness: 0.02 μm) formed of an undoped GaN, an n-type GaN layer (thickness: 4 μm) doped with silicon, and a p-type GaN layer (thickness: 5 μm) doped with magnesium, sequentially stacked in the order mentioned on a sapphire substrate. Then, the p-type GaN layer was partially etched

away to expose a portion of the surface of the n-type GaN layer.

[0092] The exposed surface portion of the n-type GaN layer was masked. Then, nickel and then gold were vapor-deposited on the entire surface of the p-type GaN layer, to a thickness of 0.03 μm, and a thickness of 0.07 μm, respectively. Then, the deposited film was masked, and aluminum was vapor-deposited on the exposed surface portion of the n-type GaN layer after removing the mask thereon.

[0093] Thereafter, the wafer thus obtained, was subjected to an annealing treatment at 500°C for 10 minutes, thereby alloying the nickel and gold, and rendering them light-transmissive. The p-electrode after the annealing had a thickness of 0.07 μm, and was light-transmissive.

[0094] The wafer, thus annealed, was cut into chips of 350 μm square. One chip was mounted on a cup-like lead frame as shown in FIG. 1, and the predetermined wire bonding operation was performed, to prepare a light-emitting diode. The light-emitting output power of this diode was 80 μW at 20 mA, and the forward voltage was 4 V.

[0095] The number of chips cut out from the wafer was about 16,000. The yield of the good quality devices obtained from these chips, excluding the contact-failure devices was 95% or more.

[0096] Meanwhile, chips were cut out from the wafer obtained in Example 1 so that the chip might be mounted on two separate lead frames, with the n-electrode and p-electrode contacted with the corresponding lead frames, respectively, i.e., with the sapphire substrate directed upward in the finished device, as in the prior art. The chip size had to be as large as 1 mm square at the minimum. The chip obtained was seated astride the two separate lead frames, and the predetermined electrode connections were performed to obtain a light-emitting diode. The light-emitting output power of this device was 40 μW at 20 mA, indicating that the light in the lateral direction was not fully available. Further, the number of chips cut out from the wafer was only 2,000, and the yield of the good quality devices obtained from these chips, excluding the contact-failure devices, was only 60%.

[0097] Thus, it was confirmed that, according to the present invention, a light-emitting device can be provided, which allows the observation of the light emitted therefrom to be made at the side of the gallium nitride-based III-V Group compound semiconductor layers, because the p-electrode of the invention can establish an ohmic contact with the p-type semiconductor layer, and is light-transmissive, effectively conducting the emitted light outside, without reducing the external quantum efficiency of the device. Further, it was confirmed that, according to the present invention, the chip size can be reduced, thus greatly increasing the productivity of the device, the yield of the devices can be enhanced, and the production costs can be reduced.

Example 2

[0098] The same procedures were followed as in Example 1, except that the annealing was performed at 600°C. The p-electrode obtained had a thickness substantially the same as that of Example 1, and was light-transmissive, similarly. Further, the light-emitting output power and the forward bias voltage of the light-emitting diode obtained were substantially the same as those of the diode of Example 1. The yield was also the same as in Example 1.

Example 3

[0099] The same procedures were followed as in Example 1, except that a 0.5 μm thick chromium layer, and then a 0.5 μm thick nickel layer were vapor-deposited on the p-type GaN layer. The p-electrode obtained had a thickness of 0.7 μm, and was similarly light-transmissive. Further, the light-emitting output power and the forward bias voltage of the light-emitting diode obtained were substantially the same as those of the diode of Example 1. The yield was also the same as in Example 1.

Example 4

[0100] The same procedures were followed as in Example 1, except that a 0.01 μm thick platinum layer, and then a 0.1 μm thick titanium layer were vapor-deposited on the p-type GaN layer. The p-electrode obtained had a thickness of 0.07 μm, and was similarly light-transmissive. Further, the light-emitting output power and the forward bias voltage of the light-emitting diode obtained were substantially the same as those of the diode of Example 1. The yield was also the same as in Example 1.

Example 5

[0101] A wafer of a double heterostructure was prepared by sequentially growing, on a sapphire substrate having a diameter of 2 inches, a GaN buffer layer, an n-type GaN layer doped with silicon, a first clad layer of GaAlN doped with silicon, an active layer of InGaN doped with zinc and silicon, a second clad layer of GaAlN doped with magnesium, and finally a contact layer of p-type GaN doped with magnesium.

[0102] Then, an etching was performed such that one chip will have the structure of FIG. 10, thus partially exposing the n-type GaN layer. By using a predetermined mask, a 10 nm thick titanium layer and then a 0.5 μm thick gold layer were formed to form a multi-layered film having a diameter of 100 μm on each exposed portion of the n-type GaN layer.

[0103] The wafer, thus obtained, was subjected to an annealing treatment at 600°C for 5 minutes under nitrogen atmosphere, thereby converting each multi-layered film into an n-electrode. The current-voltage characteristics of all n-electrode were measured with a wafer prober, and indicated the ohmic characteristics as shown in FIG. 12D.

[0104] Thereafter, a p-electrode was formed on the p-type contact layer by a conventional method, and the wafer was cut into respective chips. Thus, 15,000 chips were obtained from the 2-inch diameter wafer.

[0105] Each chip was mounted on a lead frame by the die bonding, and gold wires were bonded to the p- and n-electrodes, respectively, by the ball bonder. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at random, and the gold wire of each chip was pulled. All the gold wires were broken before peeling off the n-electrodes.

Example 6

[0106] 15,000 light-emitting chips were obtained in the same manner as in Example 5, except that a 100 angstrom titanium layer, and then a 0.4 μm thick aluminum layer were vapor-deposited as the n-electrode material. The measurement of the current-voltage characteristics on all the n-electrodes gave the characteristics shown in FIG. 11A. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at random, and the gold wire of each chip was pulled. All the gold wires were broken before peeling off the n-electrodes.

Example 7

[0107] 15,000 light-emitting chips were obtained in the same manner as in Example 5, except that a 0.5 μm thick layer of a Ti-Al alloy containing 1% by weight of titanium was vapor-deposited as the n-electrode material. The measurement of the current-voltage characteristics on all the n-electrodes with the wafer prober gave the characteristics shown in FIG. 11B. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at random, and the gold wire of each chip was pulled. All the gold wires were broken before peeling off the n-electrodes.

Example 8

[0108] The light-emitting chip of Example 5 was mounted on two separate lead frames at its p-electrode and n-electrode. The p-electrode and n-electrode were adhered to the lead frames with indium adhesives, respectively. After the bonding, the lead frames were pulled. The indium adhesive and the lead frame were separated at the interface therebetween.

[0109] This Example demonstrates that the n-electrode of the invention strongly adheres to a lead frame with a conventional adhesive, such as solder, indium, a gold alloy.

Example 9

[0110] 15,000 light-emitting chips were obtained in the same manner as in Example 5, except that a 100 angstrom thick titanium layer, and then a 0.1 μm thick aluminum layer were vapor-deposited to form a first thin film, and further a 0.1 μm thick titanium layer and then a 0.1 μm thick nickel layer were vapor-deposited as the second thin film. The measurement of the current-voltage characteristics on all the n-electrodes with the wafer prober gave the characteristics shown in FIG. 13D. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at random, and the gold wire of each chip was pulled. All the gold wires were broken before peeling off the n-electrodes.

Example 10

[0111] 15,000 light-emitting chips were obtained in the same manner as in Example 9, except that a 0.1 μm thick titanium layer, and then a 0.4 μm thick gold layer were vapor-deposited as the second thin film of the n-electrode material. The measurement of the current-voltage characteristics on all the n-electrodes with the wafer prober gave the characteristics shown in FIG. 14D. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at ramdom, and the gold wire of each chip was pulled. All the gold wires were broken before separating from the n-electrodes.

Example 11

[0112] 15,000 light-emitting chips were obtained in the same manner as in Example 9, except that a 0.1 μm thick titanium layer, then a 0.1 μm thick nickel layer, and finally a 0.4 μm thick gold layer were vapor-deposited as the second thin film of the n-electrode material. The measurement of the current-voltage characteristics on all the n-electrodes with the wafer prober gave the characteristics shown in FIG. 13C or 13D. Of the 15,000 chips, no n-electrodes were separated from the balls during the ball bonding. Further, twenty chips were sampled at random, and the gold wire of each chip was pulled. All the gold wires were broken before separating from the n-electrodes.

Example 12

[0113] The light-emitting chip of Example 9 was mounted on two separate lead frames at its p-electrode and n-electrode. The p-electrode and n-electrode were adhered to the lead frames with indium adhesives, respectively. After the adhesion, the lead frames were pulled. The indium adhesive and the lead frame were separated at the interface therebetween.

[0114] The present invention has been described with reference to specific embodiments. However, the present invention should not be limited thereto, and each embodiment may be applied to the other embodiments where appropriate. Further, the present invention can also be applied to gallium nitride-based III-V Group compound semiconductor light-emitting device of a p-n single heterostructure, in addition to gallium nitride-based III-V Group compound semiconductor light-emitting device of a p-n homojunction structure, or of a double heterostructure. In addition, the present invention may be applied to not only a light-emitting diode, but also the other light-emitting device such as a light-emitting laser diode, as well as a photodetector having the sensitivity to a wavelength of 600 nm or less, such as a solar cell or a photodiode. Furthermore, the present invention provides an electrode material which forms an ohmic contact with a gallium nitride-based III-V Group compound semiconductor, and thus can be applied to any suitable device having a p-type gallium nitride-based III-V Group compound semiconductor layer and/or an n-type gallium nitride-based III-V Group compound semiconductor layer, on a substrate. As such a substrate, not only an insulating substrate such as sapphire, but also a semiconductor substrate such as silicon carbide (SiC), silicon (Si), zinc oxide (ZnO), gallium arsenide (GaAs) or gallium phosphide (GaP) may be used.

Claims

1. A gallium nitride-based III-V group compound semiconductor device comprising:

   a substrate (11) having first (11a) and second (11b) major surfaces;
   a semiconductor stacked structure arranged over said first major surface of the substrate, and comprising an n-type gallium nitride-based III-V group compound semiconductor layer (12) and a p-type gallium nitride-based III-V group compound semiconductor layer (13);
   a first electrode (14) provided in contact with said n-type semiconductor layer (12); and
   a second electrode (15) provided in contact with said p-type semiconductor layer (13) and comprising a metallic material; **characterized in that**
   said second electrode (15) has such a thickness that said second electrode (15) is light-transmitting, and said second electrode (15) establishes ohmic contact with said p-type semiconductor layer.

2. Device according to claim 1, characterized in that the device is adapted to emit light at a side of said first major surface of the substrate (11).

3. Device according to claim 1 or 2, characterized in that said second electrode (15) is formed of a metallic material comprising at least one metal selected from the group consisting of gold, nickel, platinum, aluminum, tin, indium, chromium and titanium.

4. Device according to one of the foregoing claims, characterized in that said second electrode (15) is formed of a metallic material comprising at least two metals selected from the group consisting of chromium, nickel, gold, titanium and platinum.

5. Device according to one of the foregoing claims, characterized in that said second electrode (15) is formed of a metallic material comprising gold and nickel.

6. Device according to claim 5, characterized in that said second electrode (15) comprises a layer of nickel provided

in direct contact with said p-type layer, and a layer of gold provided on said nickel layer.

7. Device according to one of the foregoing claims, characterized in that said second electrode (15) has a thickness of 0.005 μm to 0.2 μm.

8. Device according to one of the foregoing claims, characterized by further comprising a bonding pad (17, 32) electrically connected to said second electrode (15), for bonding with a bonding wire (21).

9. Device according to claim 8, characterized in that said bonding pad (17, 32) is formed of gold or a metallic material comprising gold, and not containing aluminum or chromium.

10. Device according to claim 8, characterized in that said bonding pad (17, 32) is formed of a metallic material comprising gold and at least one metal selected from the group consisting of titanium, nickel, indium and platinum.

11. Device according to claim 8, characterized in that said bonding pad (17, 32) is formed of the same metallic material forming said second electrode (15).

12. Device according to claim 8, characterized in that said bonding pad (17, 32) comprises a layer of nickel provided in direct contact with said second electrode (15), and a layer of gold provided on said nickel layer.

13. Device according to claim 8, characterized in that said second electrode (15) has a cut-off portion exposing a part of the surface of said p-type semiconductor layer (13), and said bonding pad (32) is filled in said cut-off portion.

14. Device according to claim 13, characterized in that said bonding pad (32) is formed of a metallic material which adheres to said p-type semiconductor layer (13) more strongly than said second electrode (15).

15. Device according to claim 14, characterized in that said bonding pad (32) is formed of aluminum, or a metallic material comprising at least two metals selected from the group consistign of chrominium, aluminum and gold.

16. Device according to one of the claims 8 to 15, characterized in that said first major surface is substantially square, said bonding pad (17, 32) is arranged at a first corner portion of said second electrode (15), and said first electrode (14) is arranged on said n-type semiconductor layer (12) at a second corner portion thereof on a diagonal line of the square, including said first corner portion.

17. Device according to one of the foregoing claims, characterized by comprising a protective film (411, 412, 413) formed of a transparent and electrically insulative material, and covering said second electrode (15).

18. Device according to claim 17, characterized in that said protective film (411, 412, 413) is formed of silicon oxide, aluminum oxide, titanium oxide, or silicon nitride.

19. Device according to claim 17, characterized in that said protective film (411, 412, 413) also covers a surface of said first electrode (14).

20. Device according to one of the claims 17 to 19, characterized in that said protective film covers also said bonding pad (17).

21. A gallium nitride-based III-V group compound semiconductor device comprising:

a substrate (11) having first (11a) and second (11b) major surfaces;
a semiconductor stacked structure arranged over said first major surface of the substrate, and comprising an n-type gallium nitride-based III-V group compound semiconductor layer (12) and a p-type gallium nitride-based III-V group compound semiconductor layer (13);
a first electrode (14) provided in contact with said n-type semiconductor layer (12); and
a second electrode (15) provided in contact with said p-type semiconductor layer (13) and comprising a metallic material; characterized in that
said first electrode (14) is made of a combination of titanium with gold, or a combination with titanium with aluminum, and establishes ohmic contact with said n-type semiconductor layer (12).

22. Device according to claim 21, characterized in that said first electrode (14) consists of a layer of titanium provided in direct contact with said n-type semiconductor layer (12), and a layer of aluminum or a layer of gold, provided on said titanium layer.

23. Device according to claim 21, characterized in that said first electrode (14) consists of a layer of titanium provided in direct contact with said n-type semiconductor layer (12), a layer of aluminum provided on said titanium layer, and a layer of gold provided on said aluminum layer.

24. Device according to claim 21, characterized in that said first electrode (14) is made of the combination of titanium and aluminum, and said first electrode (14) is covered with a covering layer formed of a high-melting point metallic material having a melting point higher than aluminum.

25. Device according to claim 24, characterized in that said covering layer comprises titanium.

26. Device according to claim 24, characterized in that said covering layer comprises gold, and titanium and/or nickel.

27. Device according to one of the claims 21 to 26, characterized by further comprising a bonding pad (17, 32) electrically connected to said second electrode (15), for bonding with a bonding wire.

28. Device according to claim 27, characterized in that said first major surface (11a) is substantially square, said bonding pad (17, 32) is arranged at a first corner portion of said second electrode (15), and said first electrode (14) is arranged on said n-type semiconductor layer (12) at a second corner portion thereof on a diagonal line of the square, including said first corner portion.

29. Device according to one of the claims 21 to 28, characterized in that said second electrode (15) comrises nickel and gold.

30. A method of using a gallium nitride-based III-V group compound semiconductor device according to one of the claims 1 to 20, said method characterized by comprising:

providing a gallium nitride-based III-V group compound semiconductor device structure including a substrate (11) having first (11a) and second (11b) major surfaces, and a semiconductor stacked stucture arranged over said first major surface of the substrate, and comprising an n-type gallium nitride-based III-V group compound semiconductor layer (12) and a p-type gallium nitride-based III-V group compound semiconductor layer (13);
forming a layer of a metallic material in contact with said p-type semiconductor layer; and subjecting said metallic layer to an annealing treatment to render said metallic material light-transmissive and establish an ohmic contact with said p-type semiconductor electrode, thereby providing a light-transmitting ohmic electrode (15) in direct contact with said p-type semiconductor layer (13), wherein said annealing is conducted at a temperature of 400°C or more.

31. A method of using a gallium nitride-based III-V group compound semiconductor device according to one of the claims 21 to 29, said method characterized by comprising:

providing a gallium nitride-based III-V group compound semiconductor device structure including a substrate (11) having first (11a) and second (11b) major surfaces, and a semiconductor stacked stucture arranged over said first major surface of the substrate, and comprising an n-type gallium nitride-based III-V group compound semiconductor layer (12) and a p-type gallium nitride-based III-V group compound semiconductor layer (13);
forming a layer of a metallic material comprising titanium, and aluminum or gold in contact with said n-type semiconductor layer (12); and
subjecting said material layer to an annealing treatement to establish an ohmic contact with said n-type semiconductor electrode (14), thereby providing an ohmic electrode in direct contact with said n-type semiconductor layer (12), wherein said annealing is conducted at a temperature of 400°C or more.

Patentansprüche

1. Halbleitereinrichtung mit III-V-Verbindungshalbleitermaterial auf Galliumnitridbasis, enthaltend:

ein Substrat (11) mit einer ersten (11a) und einer zweiten (11b) Hauptoberfläche;

eine geschichtete Halbleiterstruktur, die über der ersten Hauptoberfläche des Substrats angeordnet ist und eine n-leitende III-V-Verbindungshalbleiterschicht (12) auf Galliumnitridbasis und eine p-leitende III-V-Verbindungshalbleiterschicht (13) auf Galliumnitridbasis enthält;
eine in Kontakt mit der n-leitenden Halbleiterschicht (12) vorgesehene erste Elektrode (14) und
eine in Kontakt mit der p-leitenden Halbleiterschicht (13) und einer ein metallisches Material enthaltenden zweiten Elektrode (15),
dadurch gekennzeichnet, daß
die zweite Elektrode (15) eine solche Dicke hat, daß sie lichtdurchlässig ist, und daß die zweite Elektrode (15) ohmschen Kontakt mit der p-leitenden Halbleiterschicht bildet.

2. Einrichtung nach Anspruch 1, dadurch gekennzeichnet, daß sie dazu ausgelegt ist, Licht an einer Seite der ersten Hauptoberfläche des Substrats (11) zu emittieren.

3. Einrichtung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die zweite Elektrode (15) aus einem metallischen Material gebildet ist, das mindestens ein Metall enthält, welches ausgewählt ist aus der Gruppe, die aus Gold, Nickel, Platin, Aluminium, Zinn, Indium, Chrom und Titan besteht.

4. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die zweite Elektrode (15) aus einem metallischen Material besteht, das mindestens zwei Metalle enthält, die ausgewählt sind aus der Gruppe, welche aus Chrom, Nickel, Gold, Titan und Platin besteht.

5. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die zweite Elektrode (15) aus einem metallischen Material besteht, das Gold und Nickel enthält.

6. Einrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die zweite Elektrode (15) mit einer in direktem Kontakt mit der p-leitenden Schicht vorgesehene Nickelschicht und eine auf dieser Nickelschicht vorgesehene Goldschicht enthält.

7. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die zweite Elektrode (15) eine Dicke von 0,005 μm bis 0,2 μm hat.

8. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß sie ferner eine mit der zweiten Elektrode (15) elektrisch verbundene Bondinsel (17, 32) zum Anheften eines Verbindungsdrahtes (21) enthält.

9. Einrichtung nach Anspruch 8, dadurch gekennzeichnet, daß die Bondinsel (17, 32) aus Gold oder aus einem metallischen Material gebildet ist, das Gold und kein Aluminium oder Chrom enthält.

10. Einrichtung nach Anspruch 8, dadurch gekennzeichnet, daß die Bondinsel (17, 32) aus einem metallischen Material gebildet ist, das Gold und mindestens ein Metall enthält, welches ausgewählt ist aus der Gruppe, die aus Titan, Nickel, Indium und Platin besteht.

11. Einrichtung nach Anspruch 8, dadurch gekennzeichnet, daß die Bondinsel (17, 32) aus dem gleichen metallischen Material wie die zweite Elektrode (15) gebildet ist.

12. Einrichtung nach Anspruch 8 dadurch gekennzeichnet, daß die Bondinsel (17, 32) eine in direktem Kontakt mit der zweiten Elektrode (15) vorgesehene Nickelschicht und eine auf dieser Nickelschicht vorgesehene Goldschicht enthält.

13. Einrichtung nach Anspruch 8, dadurch gekennzeichnet, daß die zweite Elektrode (15) einen Ausschnitt hat, der einen Teil der Oberfläche der p-leitenden Halbleiterschicht (13) freilegt, und daß die Bondinsel (32) in diesen Ausschnitt gefüllt ist.

14. Einrichtung nach Anspruch 13, dadurch gekennzeichnet, daß die Bondinsel (32) aus einem metallischen Material gebildet ist, das an der p-leitenden Halbleiterschicht (13) fester haftet als an der zweiten Elektrode (15).

15. Einrichtung nach Anspruch 14, dadurch gekennzeichnet, daß die Bondinsel (32) aus Aluminium oder einem metallischen Material gebildet ist, welches mindestens zwei Metalle enthält, die ausgewählt sind aus der Gruppe, welche

aus Chrom, Aluminium und Gold besteht.

16. Einrichtung nach einem der Ansprüche 8 bis 15, dadurch gekennzeichnet, daß die genannte erste Hauptoberfläche im wesentlichen rechteckig ist, daß die Bondinsel (17, 32) in einem ersten Eckbereich der zweiten Elektrode (15) angeordnet ist und daß die erste Elektrode (14) auf der n-leitenden Halbleiterschicht (12) in einem zweiten Eckbereich angeordnet ist, der auf einer den ersten Eckbereich enthaltenden diagonalen Linie des Rechtecks liegt.

17. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß sie einen Schutzfilm (411, 412, 413) enthält, der aus transparentem und elektrisch isolierendem Material gebildet ist und die zweite Elektrode (15) bedeckt.

18. Einrichtung nach Anspruch 17, dadurch gekennzeichnet, daß der Schutzfilm (411, 412, 413) aus Siliciumoxid, Aluminiumoxid, Titanoxid oder Siliciumnitrid gebildet ist.

19. Einrichtung nach Anspruch 17, dadurch gekennzeichnet, daß der Schutzfilm (411, 412, 413) auch eine Oberfläche der ersten Elektrode (14) bedeckt.

20. Einrichtung nach einem der Ansprüche 17 bis 19, dadurch gekennzeichnet, daß der Schutzfilm auch die Bondinsel (17) bedeckt.

21. Halbleitereinrichtung mit III-V-Verbindungshalbleitermaterial auf Galliumnitridbasis, enthaltend:

    ein Substrat (11) mit einer ersten (11a) und einer zweiten (11b) Hauptoberfläche;
    eine geschichtete Halbleiterstruktur, die über der ersten Hauptoberfläche des Substrats angeordnet ist und eine n-leitende Schicht (12) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis und eine p-leitende Schicht (13) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis enthält;
    eine in Kontakt mit der n-leitenden Halbleiterschicht (12) vorgesehene erste Elektrode (14) und
    eine in Kontakt mit der p-Halbleiterschicht (13) und ein metallisches Material enthaltende zweite Elektrode (15),
    dadurch gekennzeichnet, daß
    die erste Elektrode (14) aus einer Kombination von Titan mit Gold oder einer Kombination von Titan mit Aluminium besteht und ohmschen Kontakt mit der n-leitenden Halbleiterschicht (12) bildet.

22. Einrichtung nach Anspruch 21, dadurch gekennzeichnet, daß die erste Elektrode (14) aus einer in direktem Kontakt mit der n-leitenden Halbleiterschicht (12) befindlichen Titanschicht und einer auf dieser Titanschicht vorgesehenen Aluminiumschicht oder Goldschicht besteht.

23. Einrichtung nach Anspruch 21, dadurch gekennzeichnet, daß die erste Elektrode (14) aus einer in direktem Kontakt mit der n-leitenden Halbleiterschicht (12) vorgesehenen Titanschicht und einer auf der Titanschicht vorgesehenen Aluminiumschicht und einer auf der Aluminiumschicht vorgesehenen Goldschicht besteht.

24. Einrichtung nach Anspruch 21, dadurch gekennzeichnet, daß die erste Elektrode (14) aus der Kombination von Titan und Aluminium besteht und daß die erste Elektrode (14) mit einer Deckschicht versehen ist, die aus einem hochschmelzenden metallischen Material gebildet ist, dessen Schmelzpunkt höher liegt als derjenige von Aluminium.

25. Einrichtung nach Anspruch 24, dadurch gekennzeichnet, daß die Deckschicht Titan enthält.

26. Einrichtung nach Anspruch 24, dadurch gekennzeichnet, daß die Deckschicht Gold und Titan und/oder Nickel enthält.

27. Einrichtung nach einem der Ansprüche 21 bis 26, dadurch gekennzeichnet, daß sie ferner eine Bondinsel (17, 32) enthält, die zum Anheften eines Verbindungsdrahtes elektrisch mit der zweiten Elektrode (15) verbunden ist.

28. Einrichtung nach Anspruch 27, dadurch gekennzeichnet, daß die genannte erste Hauptoberfläche (11a) im wesentlichen rechteckig ist, daß die Bondinsel (17, 32) in einem ersten Eckbereich der zweiten Elektrode (15) angeordnet ist und daß die erste Elektrode (14) auf der n-leitenden Halbleiterschicht (12) in einem zweiten Eckbereich angeordnet ist, der auf einer den ersten Eckbereich enthaltenden diagonalen Linie des Rechtecks liegt.

29. Einrichtung nach einem der Ansprüche 21 bis 28, dadurch gekennzeichnet, daß die zweite Elektrode (15) Nickel und Gold enthält.

30. Verfahren des Verwendens einer Halbleitereinrichtung mit III-V-Verbindungshalbleitermaterial auf Galliumnitridbasis nach einem der Ansprüche 1 bis 20, wobei dieses Verfahren gekennzeichnet ist durch:

    Bereitstellung einer Struktur einer III-V-Verbindungshalbleitereinrichtung auf Galliumnitridbasis mit einem eine erste (11a) und eine zweite (11b) Hauptoberfläche aufweisenden Substrat und einer geschichteten Halbleiterstruktur, die über der ersten Hauptoberfläche des Substrats angeordnet ist und eine n-leitende Schicht (12) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis und eine p-leitende Schicht (13) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis enthält;
    Bildung einer Schicht eines metallischen Materials in Kontakt mit der p-leitenden Halbleiterschicht und Wärmebehandlung dieser metallischen Schicht, um das genannte metallische Material lichtdurchlässig zu machen und einen ohmschen Kontakt mit der p-leitenden Halbleiterelektrode herzustellen und dadurch eine lichtdurchlässige ohmsche Elektrode (15) in direktem Kontakt mit der p-leitenden Halbleiterschicht (13) zu schaffen, wobei die Wärmebehandlung auf einer Temperatur von 400°C oder höher durchgeführt wird.

31. Verfahren des Verwendens einer Halbleitereinrichtung mit III-V-Verbindungshalbleitermaterial auf Galliumnitridbasis nach einem der Ansprüche 21 bis 29, wobei das Verfahren gekennzeichnet ist durch:

    Bereitstellung einer Struktur einer III-V-Verbindungshalbleitereinrichtung auf Galliumnitridbasis mit einem eine erste (11a) und eine zweite (11b) Hauptoberfläche aufweisenden Substrat (11) und einer geschichteten Halbleiterstruktur, die über der ersten Hauptoberfläche des Substrats angeordnet ist und eine n-leitende Schicht (12) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis und eine p-leitende Schicht (13) eines III-V-Verbindungshalbleiters auf Galliumnitridbasis enthält;
    Bildung einer Schicht eines metallischen Materials, das Titan und Aluminium oder Gold enthält, in Kontakt mit der n-leitenden Halbleiterschicht (12), und
    Wärmebehandlung dieser Materialschicht zum Herstellen eines ohmschen Kontakts mit der n-leitenden Halbleiterelektrode (14), um so eine ohmsche Elektrode in direktem Kontakt mit der n-leitenden Halbleiterschicht (12) zu bilden, wobei die Wärmebehandlung auf einer Temperatur von 400°C oder höher durchgeführt wird.

Revendications

1. Dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium, comprenant :

    un substrat (11) présentant des première (11a) et seconde (11b) surfaces principales ;
    une structure de semi-conducteur superposée disposée sur ladite surface principale du substrat et comprenant une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type n (12) et une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type p (13) ;
    une première électrode (14) prévue en contact avec ladite couche de semi-conducteur de type n (12) ; et
    une seconde électrode (15) prévue en contact avec ladite couche de semi-conducteur de type p (13) et comprenant un matériau métallique ;
    caractérisé en ce que ladite seconde électrode (15) présente une épaisseur telle que ladite seconde électrode (15) est apte à transmettre la lumière et ladite seconde électrode (15) établit un contact ohmique avec ladite couche de semi-conducteur de type p.

2. Dispositif selon la revendication 1, caractérisé en ce que le dispositif est adapté pour émettre la lumière d'un côté de ladite surface principale du substrat (11).

3. Dispositif selon la revendication 1 ou 2, caractérisé en ce que ladite seconde électrode (15) est formée d'un matériau métallique comprenant au moins un métal sélectionné dans le groupe composé d'or, de nickel, de platine, d'aluminium, d'étain, d'indium, de chrome et de titane.

4. Dispositif selon l'une des revendications précédentes, caractérisé en ce que ladite seconde électrode (15) est formée d'un matériau métallique comprenant au moins deux métaux sélectionnés dans le groupe composé de chrome, de nickel, d'or, de titane et de platine.

5. Dispositif selon l'une des revendications précédentes, caractérisé en ce que ladite seconde électrode (15) est for-

mée d'un matériau métallique comprenant de l'or et du nickel.

6. Dispositif selon la revendication 5, caractérisé en ce que ladite seconde électrode (15) comprend une couche de nickel prévue en contact direct avec ladite couche de type p, et une couche d'or, prévue sur ladite couche de nickel.

7. Dispositif selon l'une des revendications précédentes, caractérisé en ce que ladite seconde électrode (15) présente une épaisseur de 0,005 µm à 0,2 µm.

8. Dispositif selon l'une des revendications précédentes, caractérisé en ce qu'il comprend en outre un plot de connexion (17, 32), connecté électriquement à ladite seconde électrode (15) pour la connexion à un fil de connexion (21).

9. Dispositif selon la revendication 8, caractérisé en ce que ledit plot de connexion (17, 32) est formé d'or ou d'un matériau métallique comprenant de l'or et ne contenant ni aluminium, ni chrome.

10. Dispositif selon la revendication 8, caractérisé en ce que ledit plot de connexion (17, 32) est formé d'un matériau métallique comprenant de l'or et au moins un métal sélectionné dans le groupe composé de titane, de nickel, d'indium et de platine.

11. Dispositif selon la revendication 8, caractérisé en ce que ledit plot de connexion (17, 32) est formé du même matériau métallique que celui formant ladite seconde électrode (15).

12. Dispositif selon la revendication 8, caractérisé en ce que ledit plot de connexion (17, 32) comprend une couche de nickel prévue en contact direct avec ladite seconde électrode (15) et une couche d'or prévue sur ladite couche de nickel.

13. Dispositif selon la revendication 8, caractérisé en ce que ladite seconde électrode (15) comporte une partie découpée exposant une partie de la surface de ladite couche de semi-conducteur de type p (13) et en ce que ledit plot de connexion (32) remplit ladite partie découpée.

14. Dispositif selon la revendication 13, caractérisé en ce que ledit plot de connexion (32) est formé d'un matériau métallique qui adhère à ladite couche de semi-conducteur de type p (13) plus fortement que ladite seconde électrode (15).

15. Dispositif selon la revendication 14, caractérisé en ce que ledit plot de connexion (32) est formé d'aluminium ou d'un matériau métallique comprenant au moins deux métaux sélectionnés dans le groupe composé de chrome, d'aluminium et d'or.

16. Dispositif selon l'une des revendications 8 à 15, caractérisé en ce que ladite première surface principale est essentiellement carrée, ledit plot de connexion (17, 32) est disposé en une première partie de coin de ladite seconde électrode (15) et en ce que ladite première électrode (14) est disposée sur ladite couche de semi-conducteur de type n (12) en une seconde partie de coin de celle-ci sur une ligne diagonale du carré, y compris ladite première partie de coin.

17. Dispositif selon l'une des revendications précédentes, caractérisé en ce qu'il comprend une pellicule de protection (411, 412, 413) formée d'un matériau transparent et électriquement isolant et qui recouvre ladite seconde électrode (15).

18. Dispositif selon la revendication 17, caractérisé en ce que ladite pellicule de protection (411, 412, 413) est formée d'oxyde de silicium, d'oxyde d'aluminium, d'oxyde de titane ou de nitrure de silicium.

19. Dispositif selon la revendication 17, caractérisé en ce que ladite pellicule de protection (411, 412, 413) recouvre également une surface de ladite première électrode (14).

20. Dispositif selon l'une des revendications 17 à 19, caractérisé en ce que ladite pellicule de protection recouvre également ledit plot de connexion (17).

21. Dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium, comprenant :

un substrat (11) présentant des première (11a) et seconde (11b) surfaces principales ;
une structure de semi-conducteur superposée disposée sur ladite première surface principale du substrat et comprenant une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type n (12) et une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type p (13) ;
une première électrode (14) prévue en contact avec ladite couche de semi-conducteur de type n (12) ; et
une seconde électrode (15) prévue en contact avec ladite couche de semi-conducteur de type p (13) et comprenant un matériau métallique ;
caractérisé en ce que ladite première électrode (14) est formée d'une combinaison de titane et d'or, ou d'une combinaison de titane et d'aluminium et établit un contact ohmique avec ladite couche de semi-conducteur de type n (12).

22. Dispositif selon la revendication 21, caractérisé en ce que ladite première électrode (14) est formée d'une couche de titane prévue en contact direct avec ladite couche de semi-conducteur de type n (12) et d'une couche d'aluminium ou d'une couche d'or, prévue sur ladite couche de titane.

23. Dispositif selon la revendication 21, caractérisé en ce que ladite première électrode (14) est formée d'une couche de titane prévue en contact direct avec ladite couche de semi-conducteur de type n (12) et d'une couche d'aluminium prévue sur ladite couche de titane et d'une couche d'or, prévue sur ladite couche d'aluminium.

24. Dispositif selon la revendication 21, caractérisé en ce que ladite première électrode (14) est formée d'une combinaison de titane et d'aluminium et en ce que ladite première électrode (14) est recouverte d'une couche couvrante formée d'un matériau métallique à haut point de fusion présentant un point de fusion supérieur à celui de l'aluminium.

25. Dispositif selon la revendication 24, caractérisé en ce que ladite couche couvrante comprend du titane.

26. Dispositif selon la revendication 24, caractérisé en ce que ladite couche couvrante comprend de l'or, et du titane et/ou du nickel.

27. Dispositif selon l'une des revendications 21 à 26, caractérisé en ce qu'il comprend en outre un plot de connexion (17, 32) connecté électriquement à ladite seconde électrode (15) pour la connexion à un fil de connexion.

28. Dispositif selon la revendication 27, caractérisé en ce que ladite première surface principale (11a) est essentiellement carrée, ledit plot de connexion (17, 32) est disposé en une première partie de coin de ladite seconde électrode (15) et en ce que ladite première électrode (14) est disposée sur ladite couche de semi-conducteur de type n (12) en une seconde partie de coin de celle-ci sur une ligne diagonale du carré, y compris ladite première partie de coin.

29. Dispositif selon l'une des revendications 21 à 28, caractérisé en ce que ladite seconde électrode (15) comprend du nickel et de l'or.

30. Procédé d'utilisation d'un dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium, selon l'une des revendications 1 à 20, ledit procédé étant caractérisé par les étapes consistant à :

prévoir une structure de dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium comprenant un substrat (11) présentant des première (11a) et seconde (11b) surfaces principales et une structure de semi-conducteur superposée disposée sur ladite surface principale du substrat et comprenant une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type n (12) et une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type p (13) ;
former une couche d'un matériau métallique en contact avec ladite couche de semi-conducteur de type p ; et
soumettre ladite couche métallique à un traitement de recuit pour rendre ledit matériau métallique apte à transmettre la lumière et établir un contact ohmique avec ladite électrode de semi-conducteur de type p, fournissant ce faisant une électrode ohmique apte à transmettre la lumière (15) en contact direct avec ladite couche de semi-conducteur de type p (13), dans lequel procédé ledit recuit est réalisé à une température de 400 °C ou plus.

31. Procédé d'utilisation d'un dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium, selon l'une des revendications 21 à 29, ledit procédé étant caractérisé par les étapes consistant à :

prévoir une structure de dispositif semi-conducteur composé de groupe III-V à base de nitrure de gallium comprenant un substrat (11) présentant des première (11a) et seconde (11b) surfaces principales et une structure de semi-conducteur superposée disposée sur ladite surface principale du substrat et comprenant une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type n (12) et une couche de semi-conducteur composé de groupe III-V à base de nitrure de gallium de type p (13) ;

former une couche d'un matériau métallique comprenant du titane et de l'aluminium ou de l'or, en contact avec ladite couche de semi-conducteur de type n (12) ; et

soumettre ladite couche de matériau à un traitement de recuit pour établir un contact ohmique avec ladite électrode de semi-conducteur de type n (14), fournissant ce faisant une électrode ohmique en contact direct avec ladite couche de semi-conducteur de type n (12), dans lequel procédé ledit recuit est réalisé à une température de 400 °C ou plus.

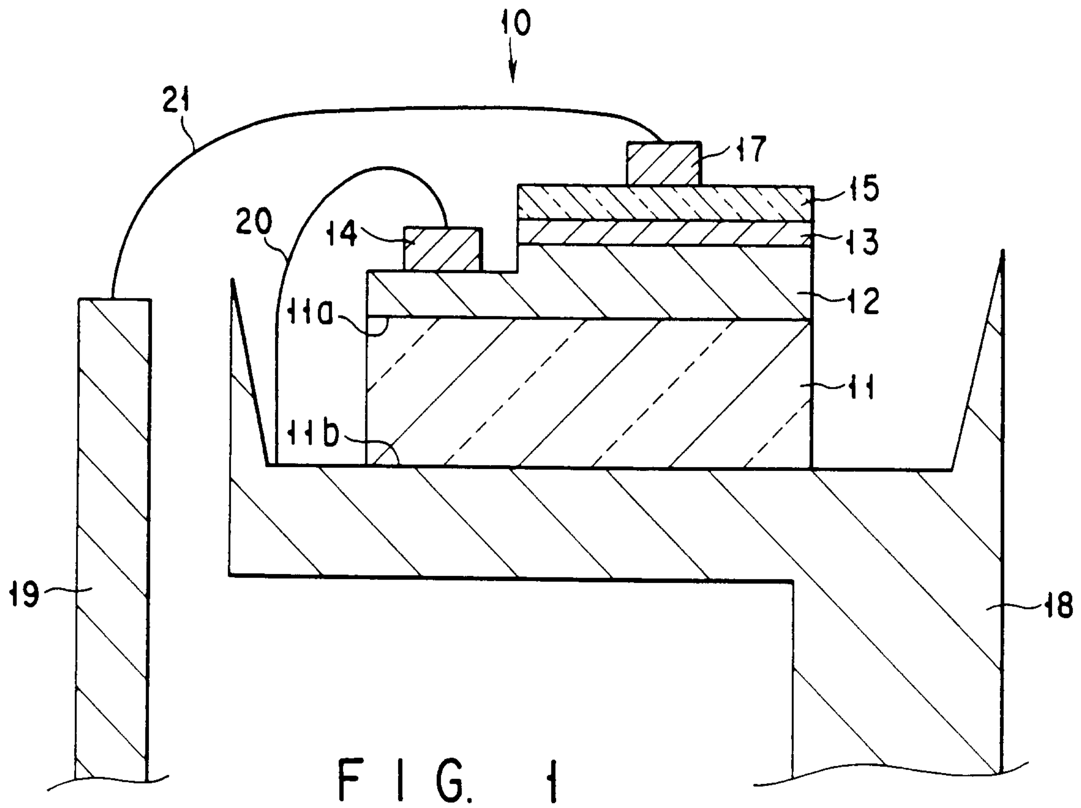

FIG. 1

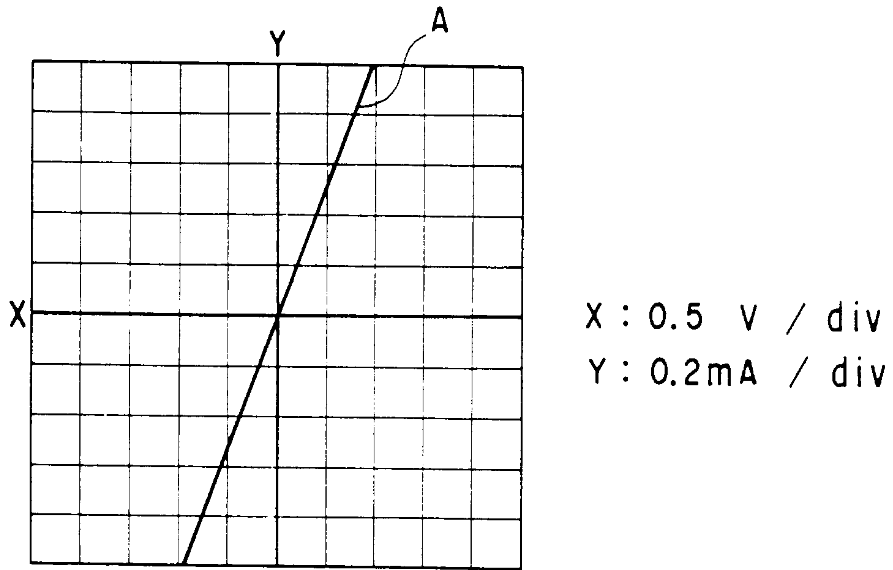

FIG. 2

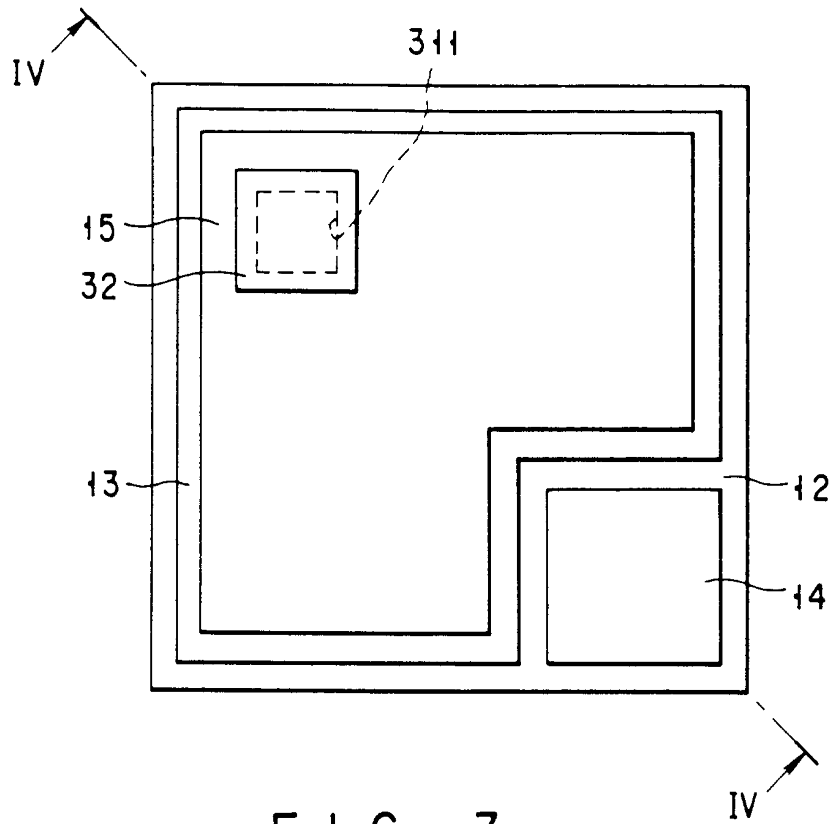

FIG. 3

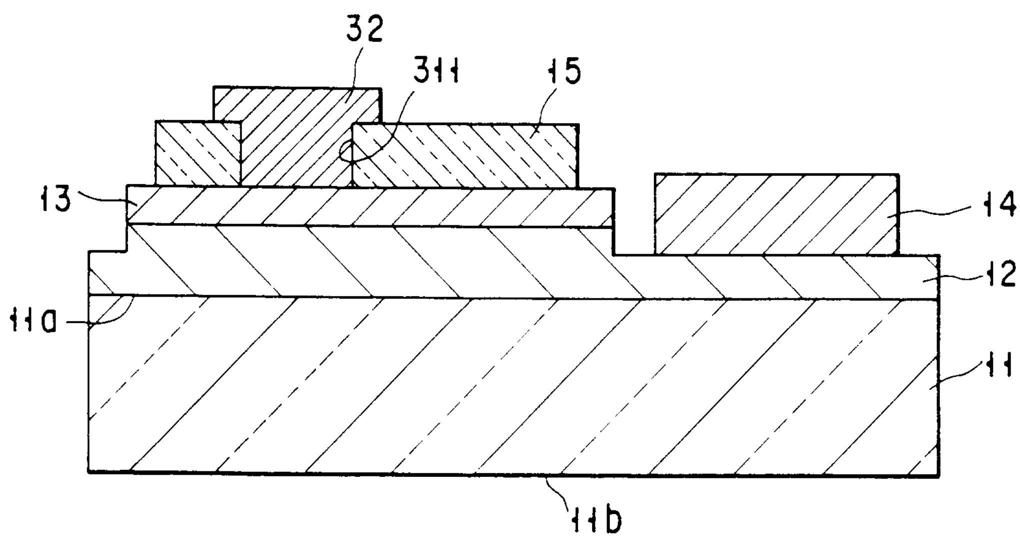

FIG. 4

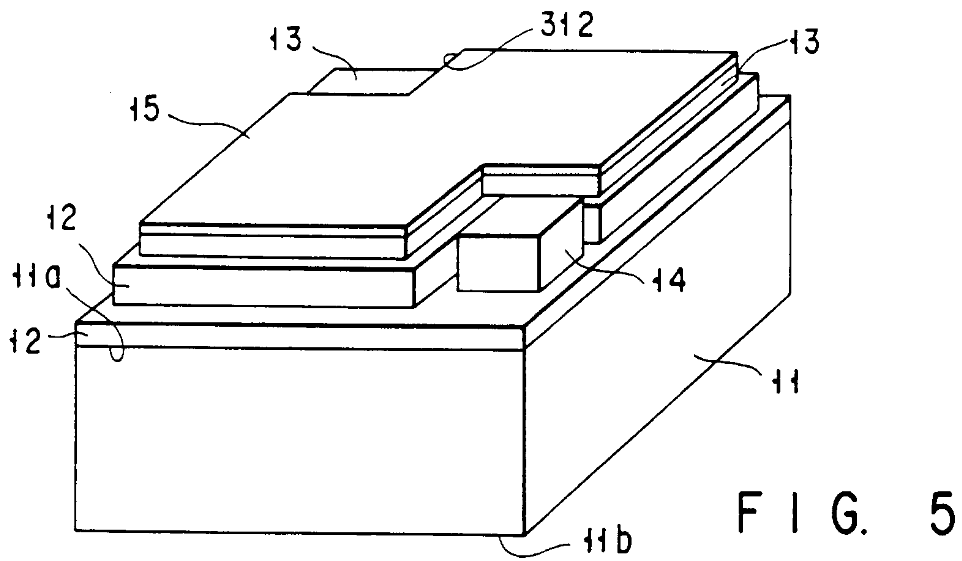

FIG. 5

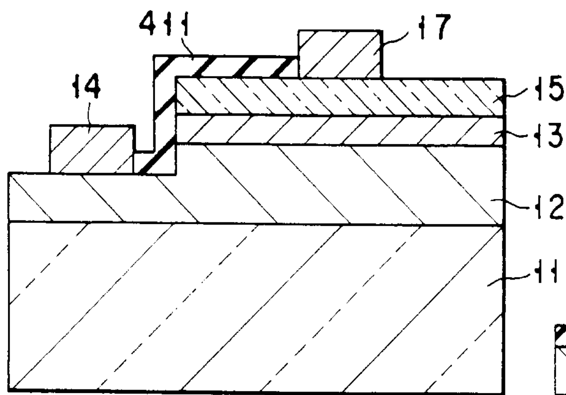

FIG. 6

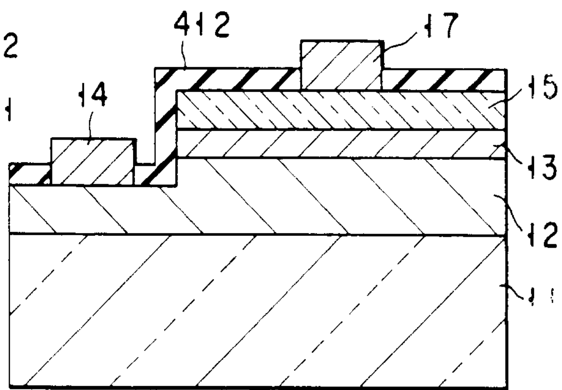

FIG. 7

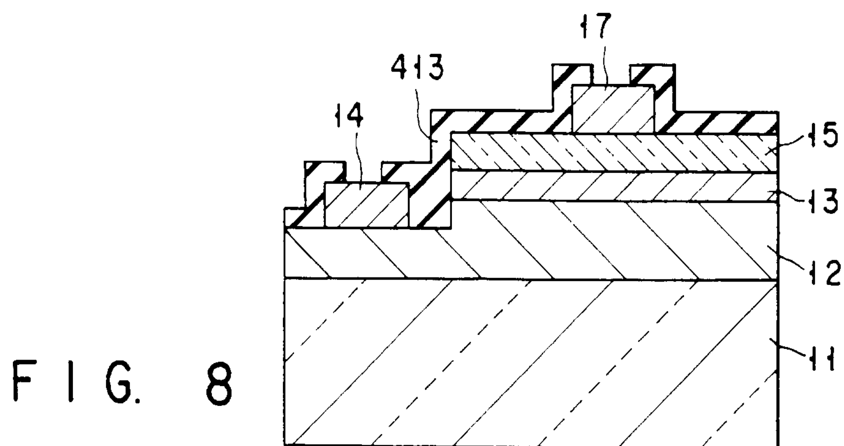

FIG. 8

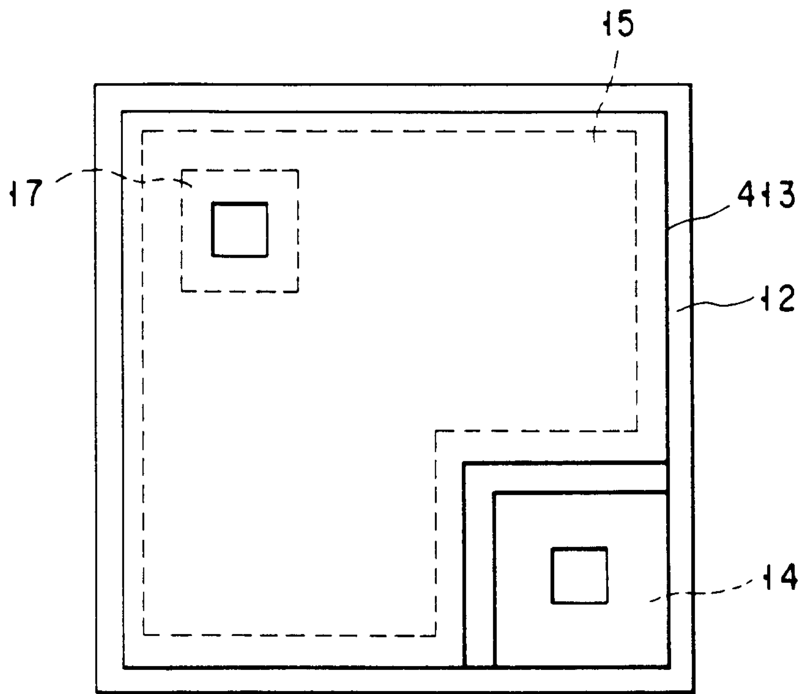

FIG. 9

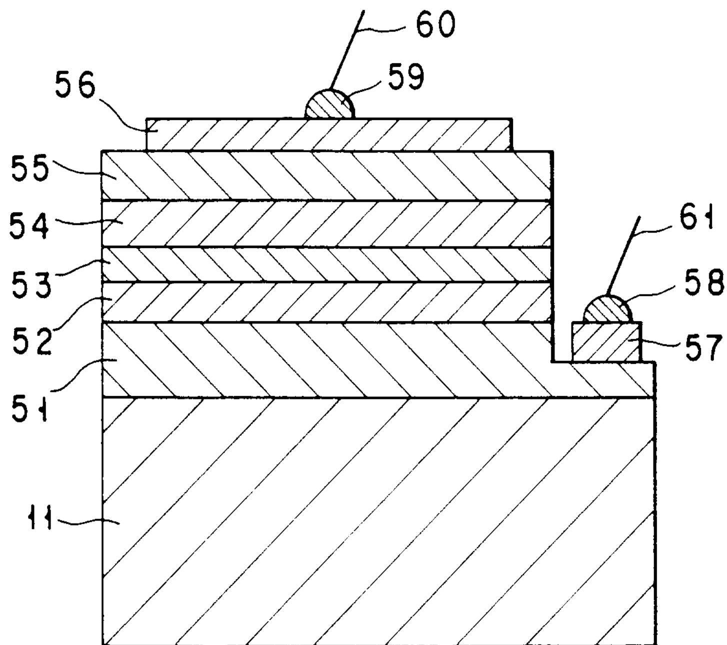

FIG. 10

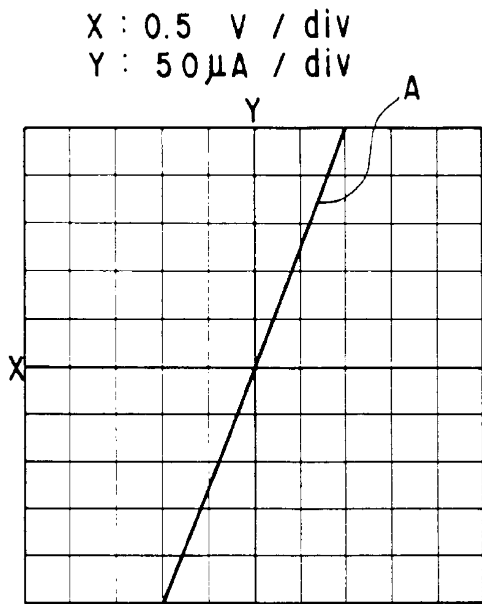

FIG. 11A

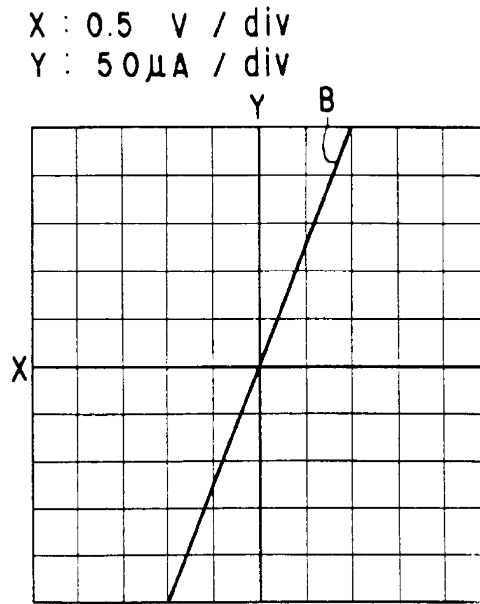

FIG. 11B

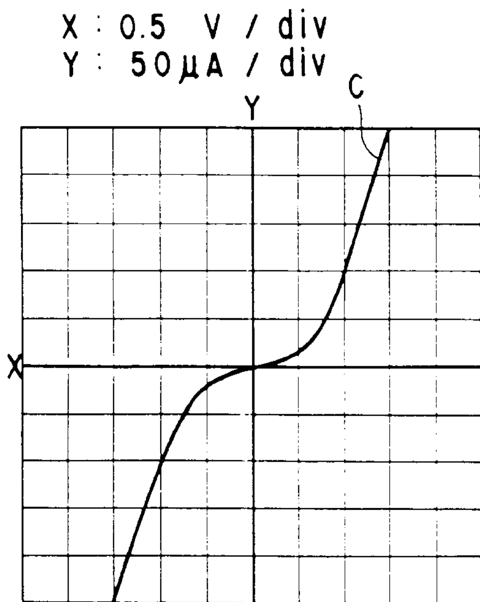

FIG. 11C

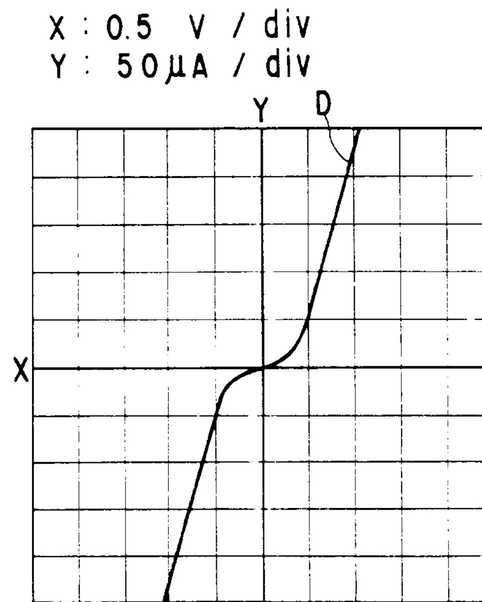

FIG. 11D

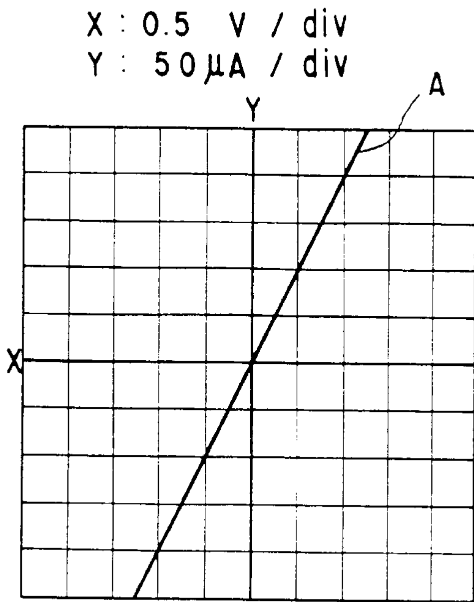

FIG. 12A

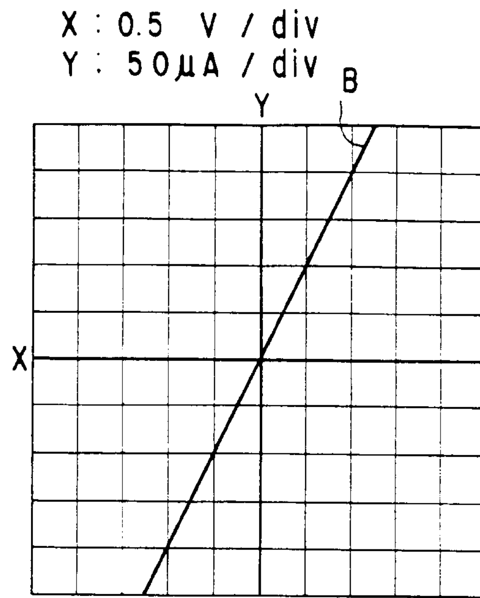

FIG. 12B

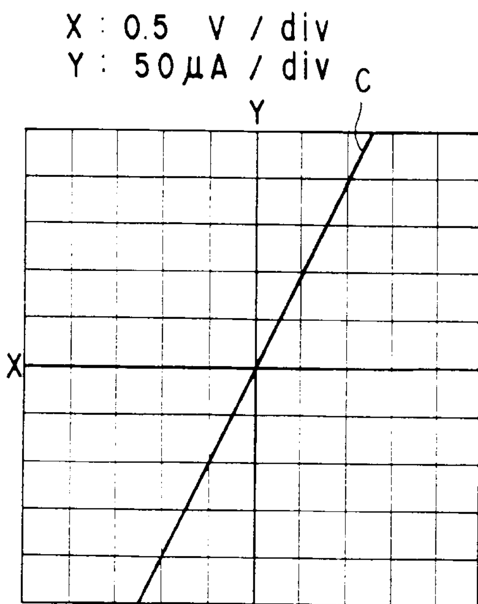

FIG. 12C

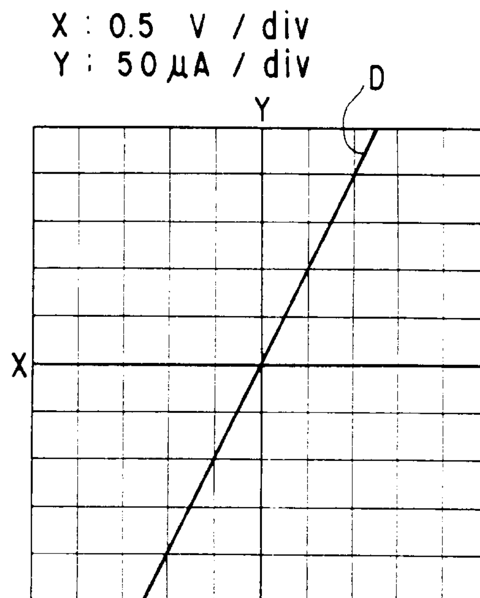

FIG. 12D

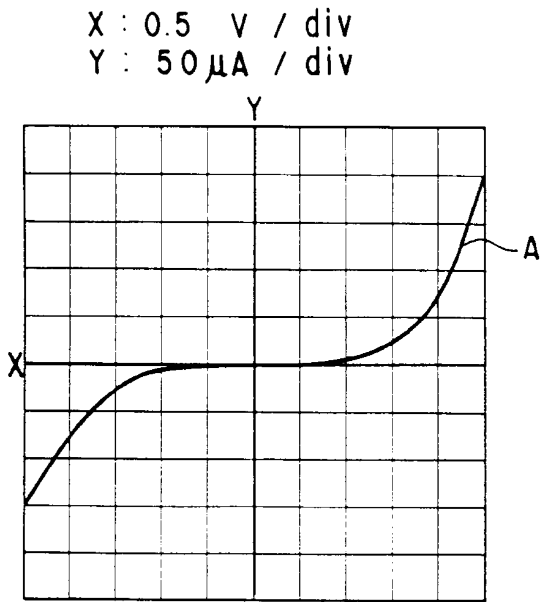

FIG. 13A

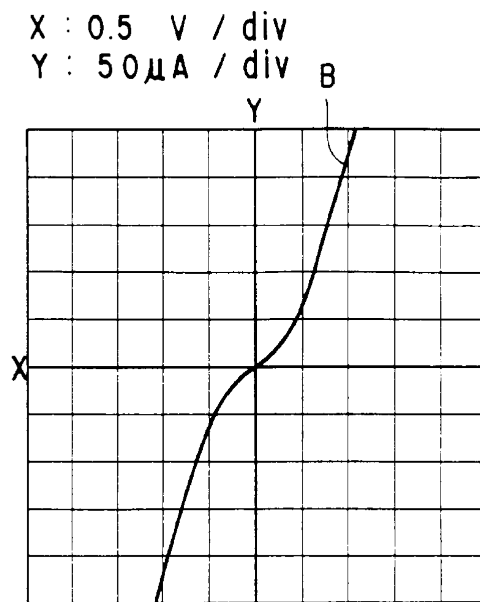

FIG. 13B

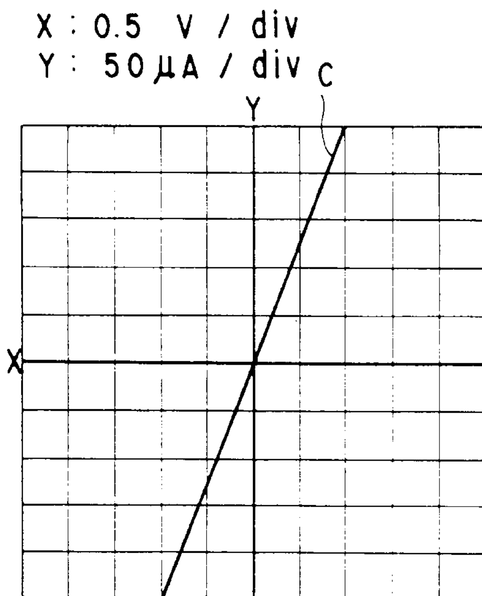

FIG. 13C

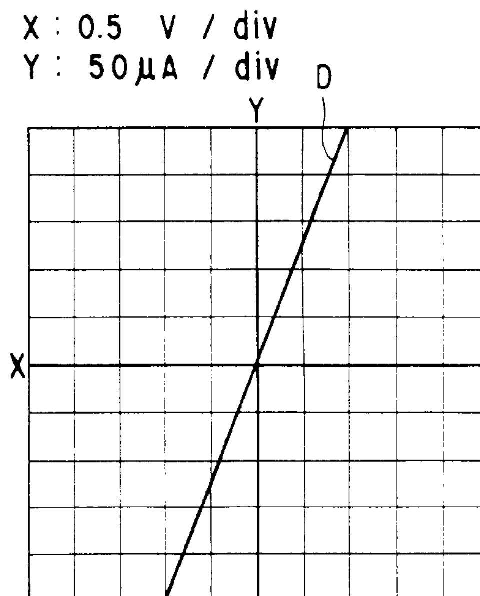

FIG. 13D

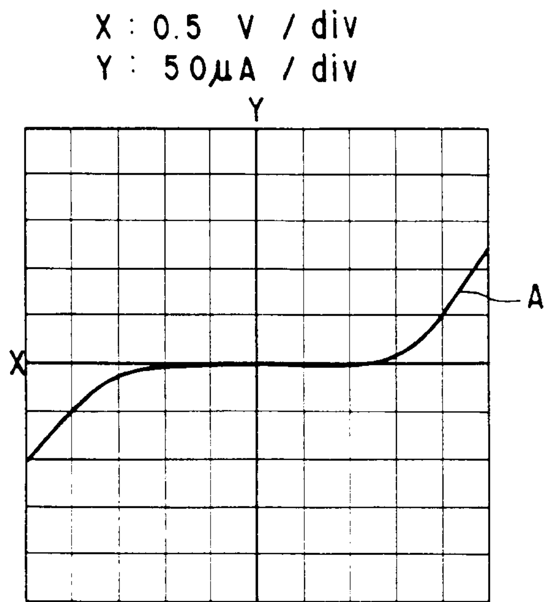

FIG. 14A

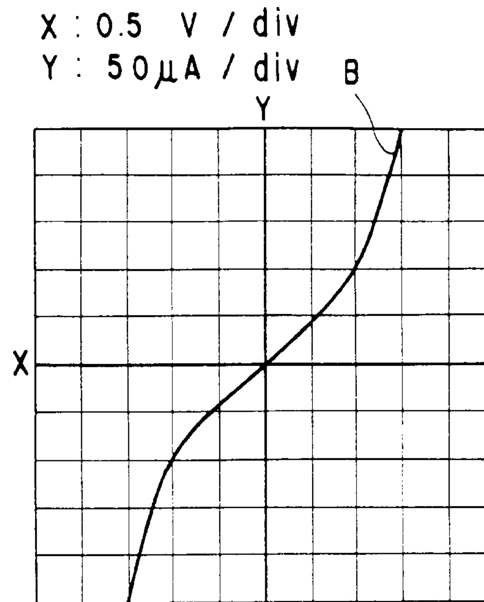

FIG. 14B

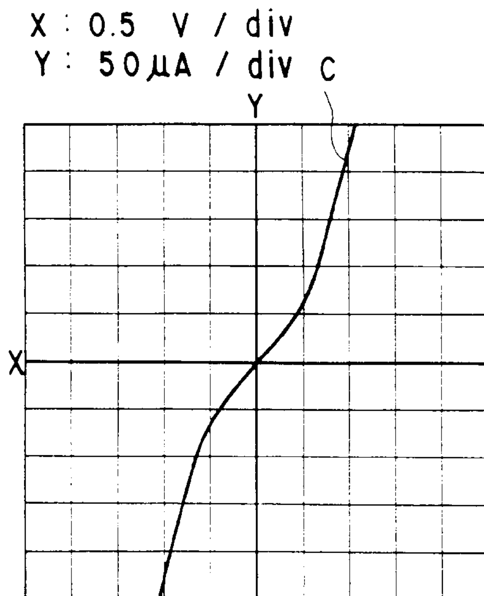

FIG. 14C

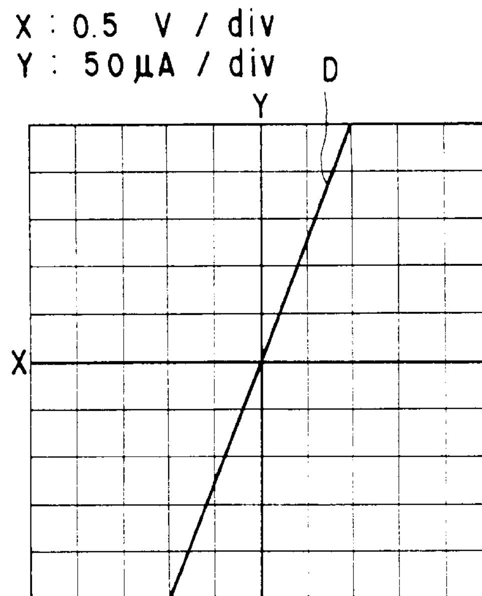

FIG. 14D

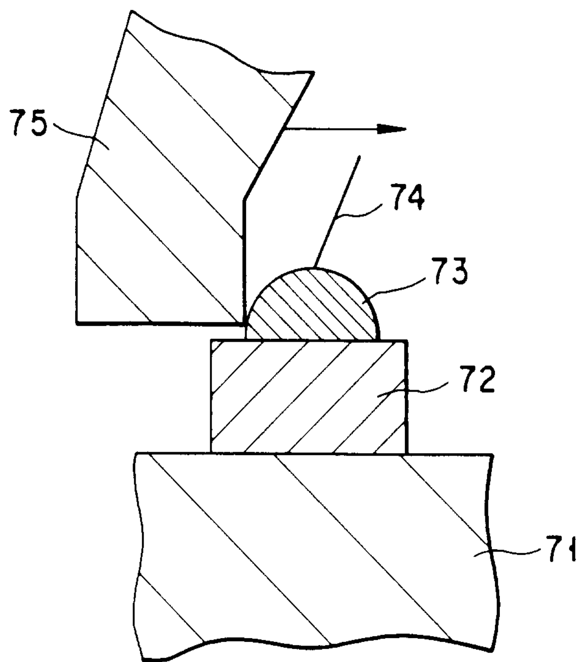

FIG. 15

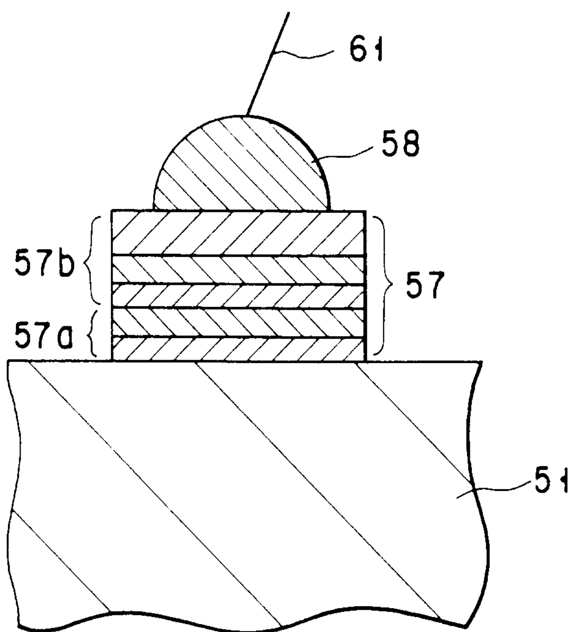

FIG. 16

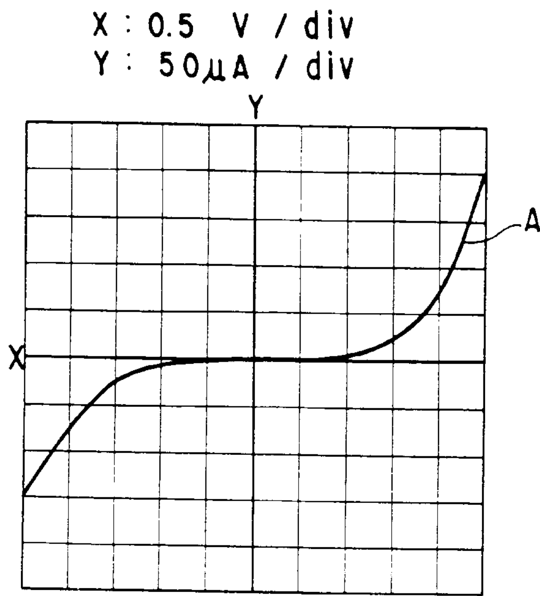

FIG. 17A

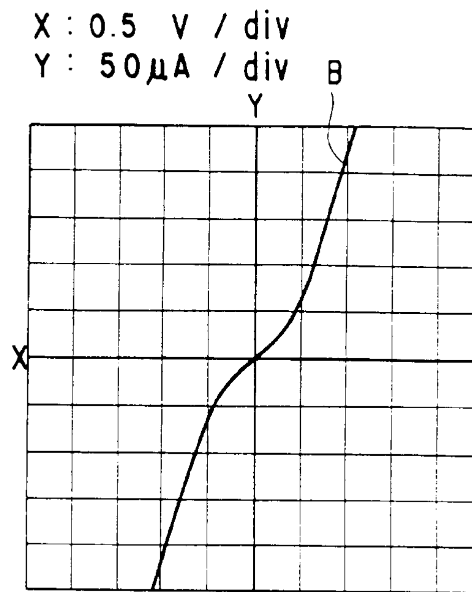

FIG. 17B

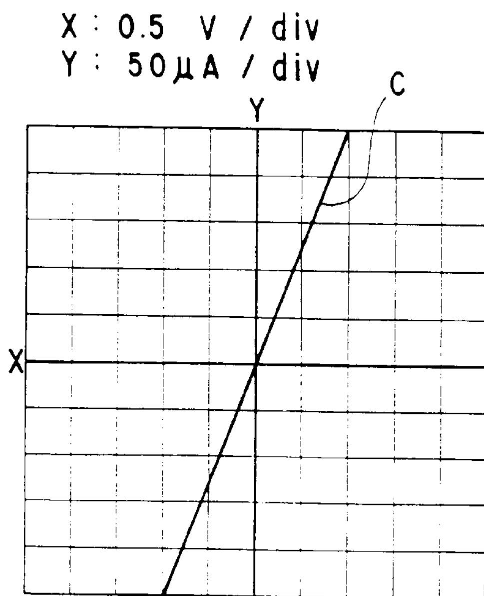

FIG. 17C

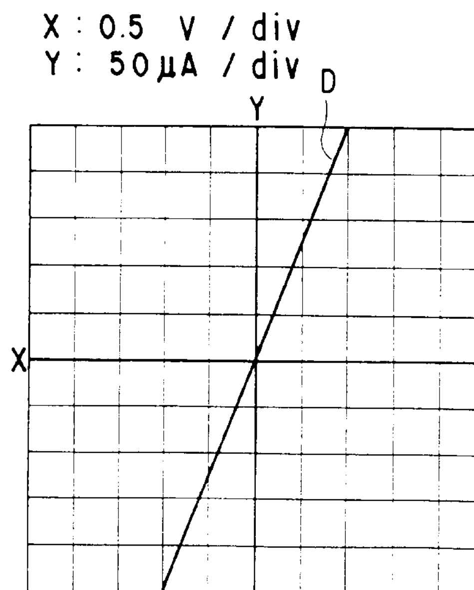

FIG. 17D